

FIG. 2

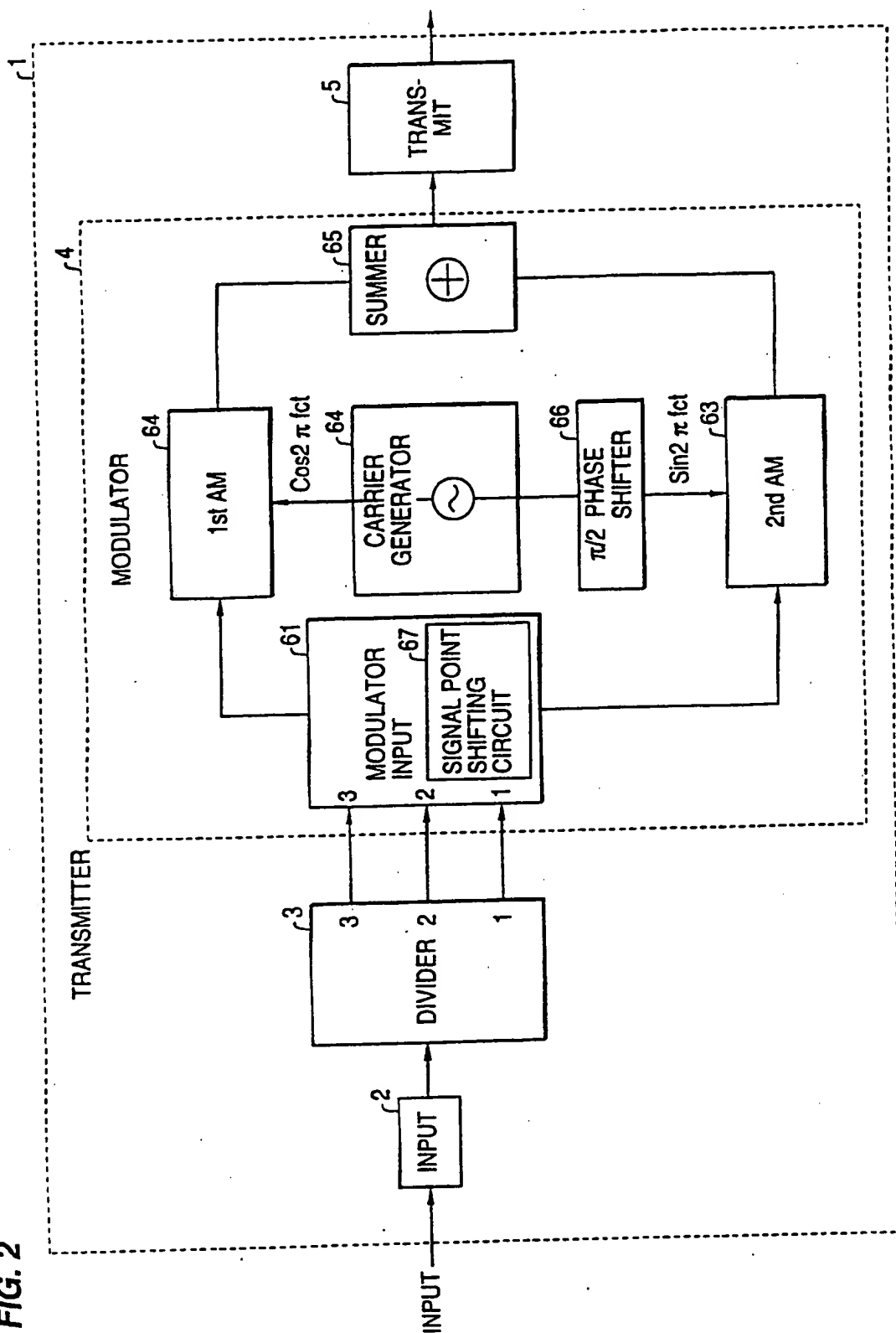




FIG. 4

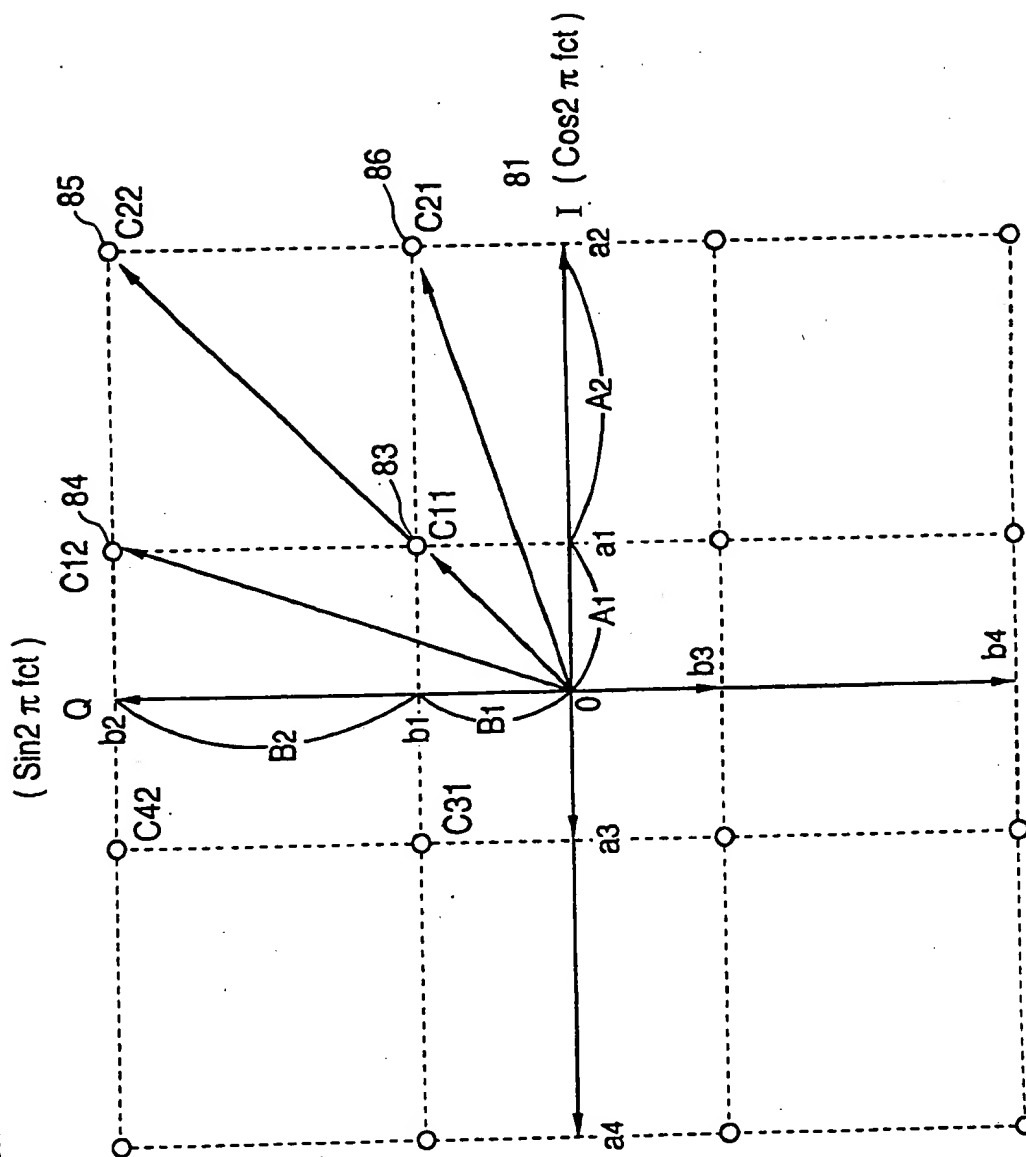


FIG. 5

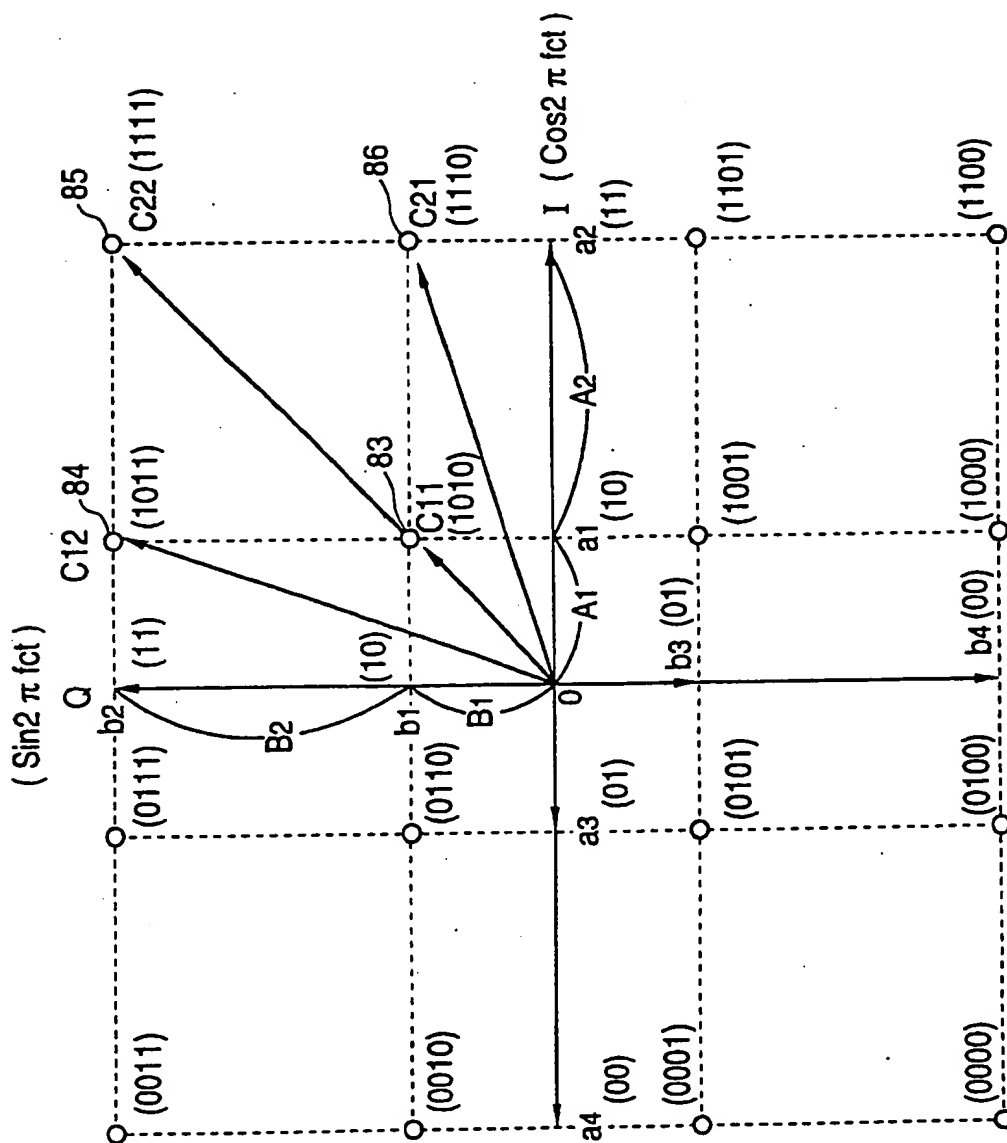


FIG. 6

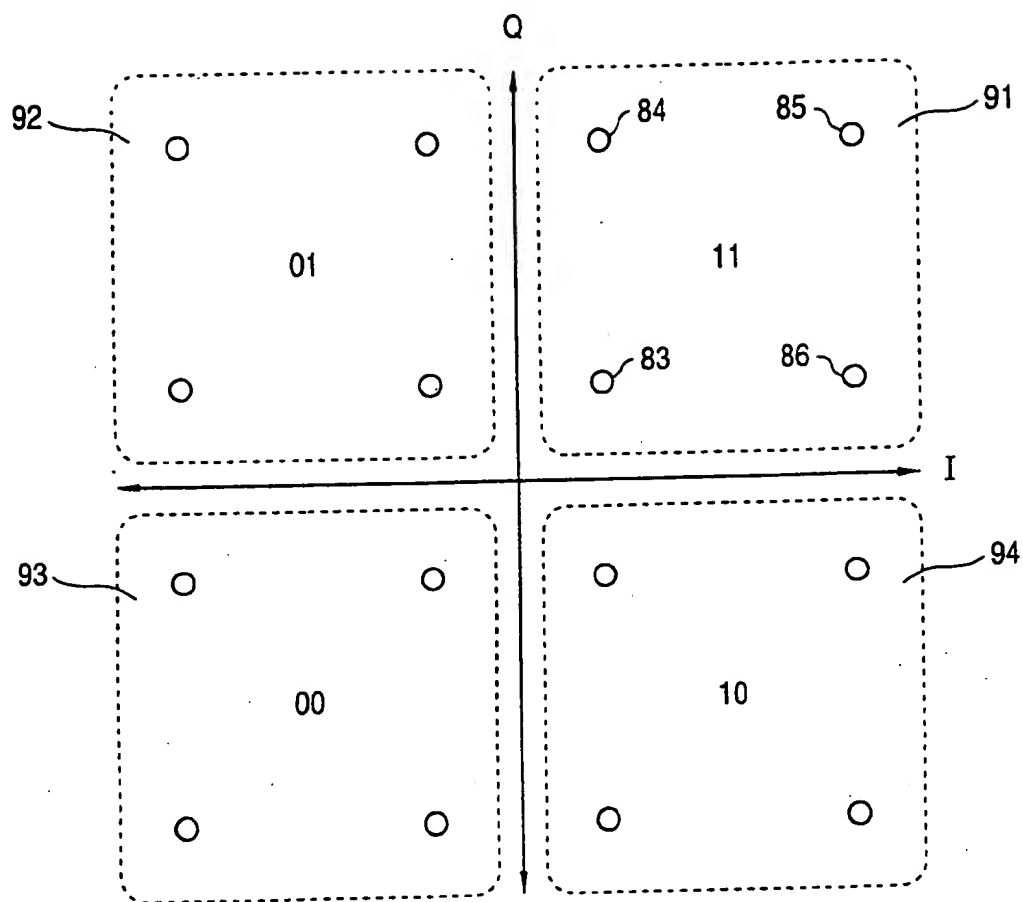


FIG. 7

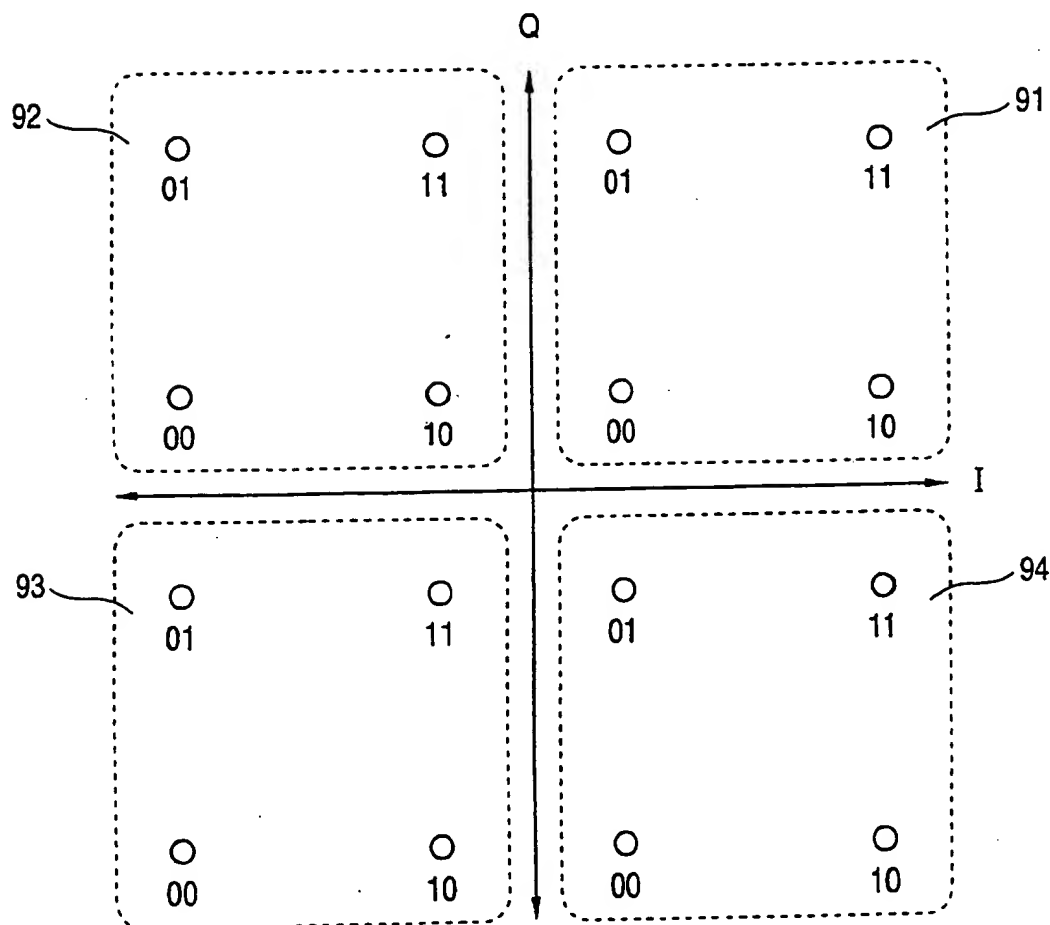


FIG. 8

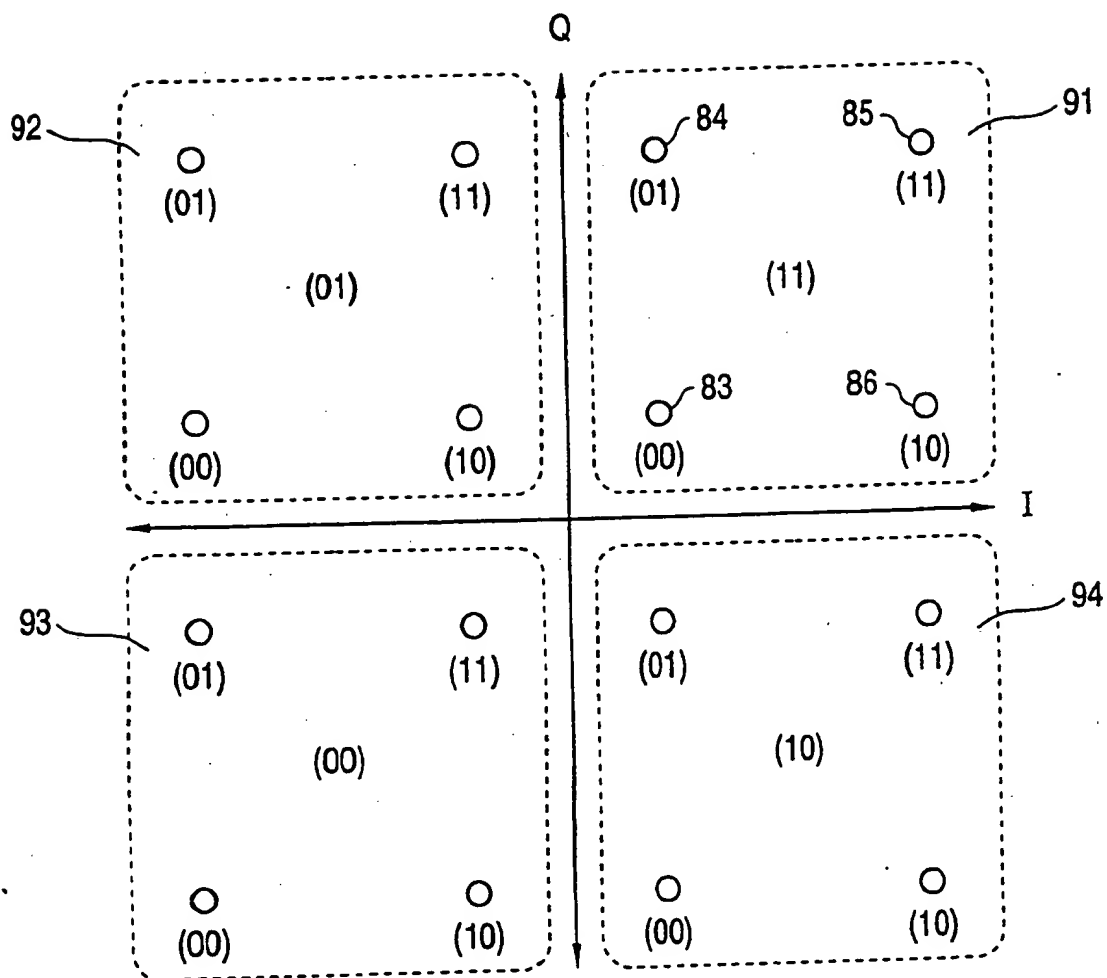
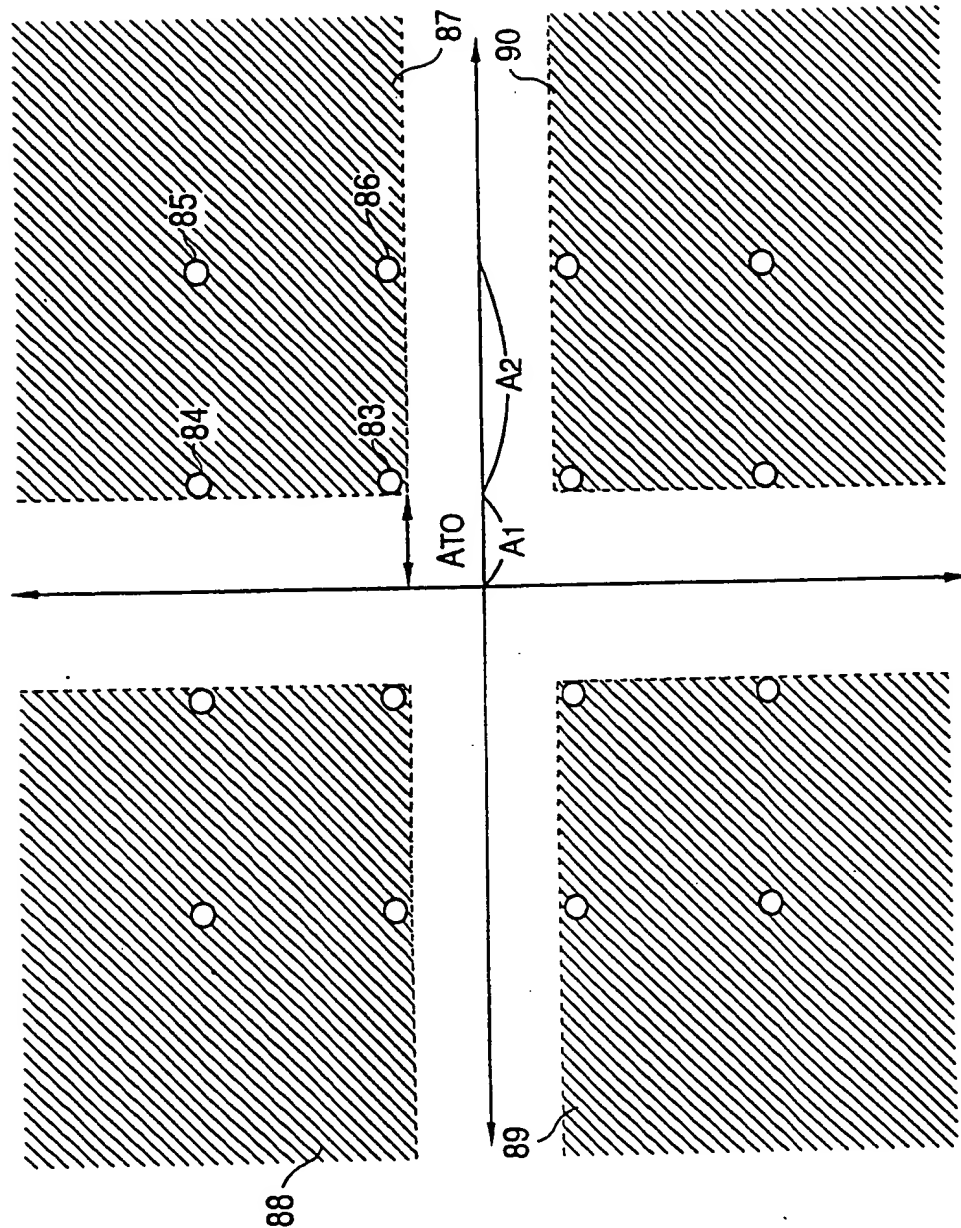


FIG. 9



**FIG. 10**

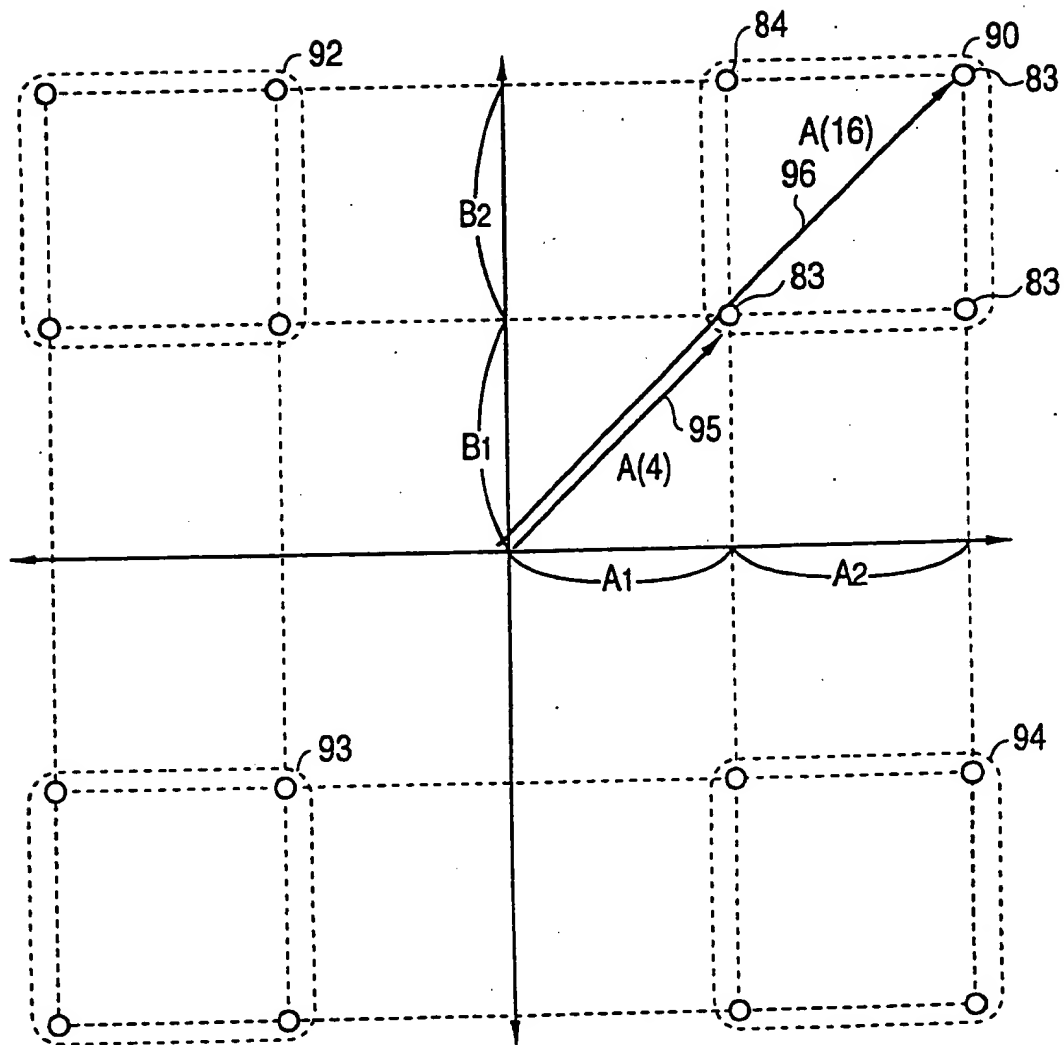


FIG. 11

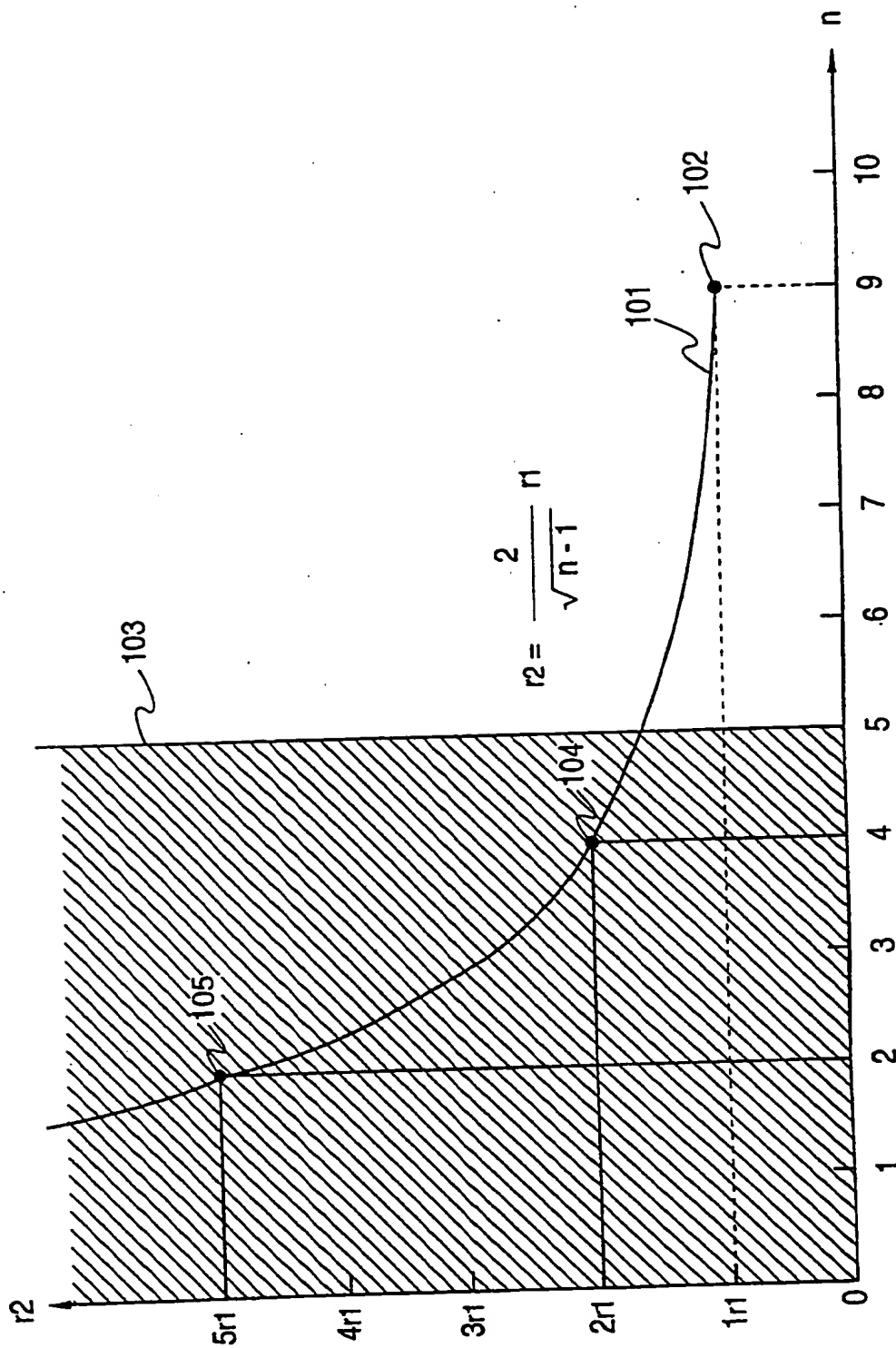


FIG. 12

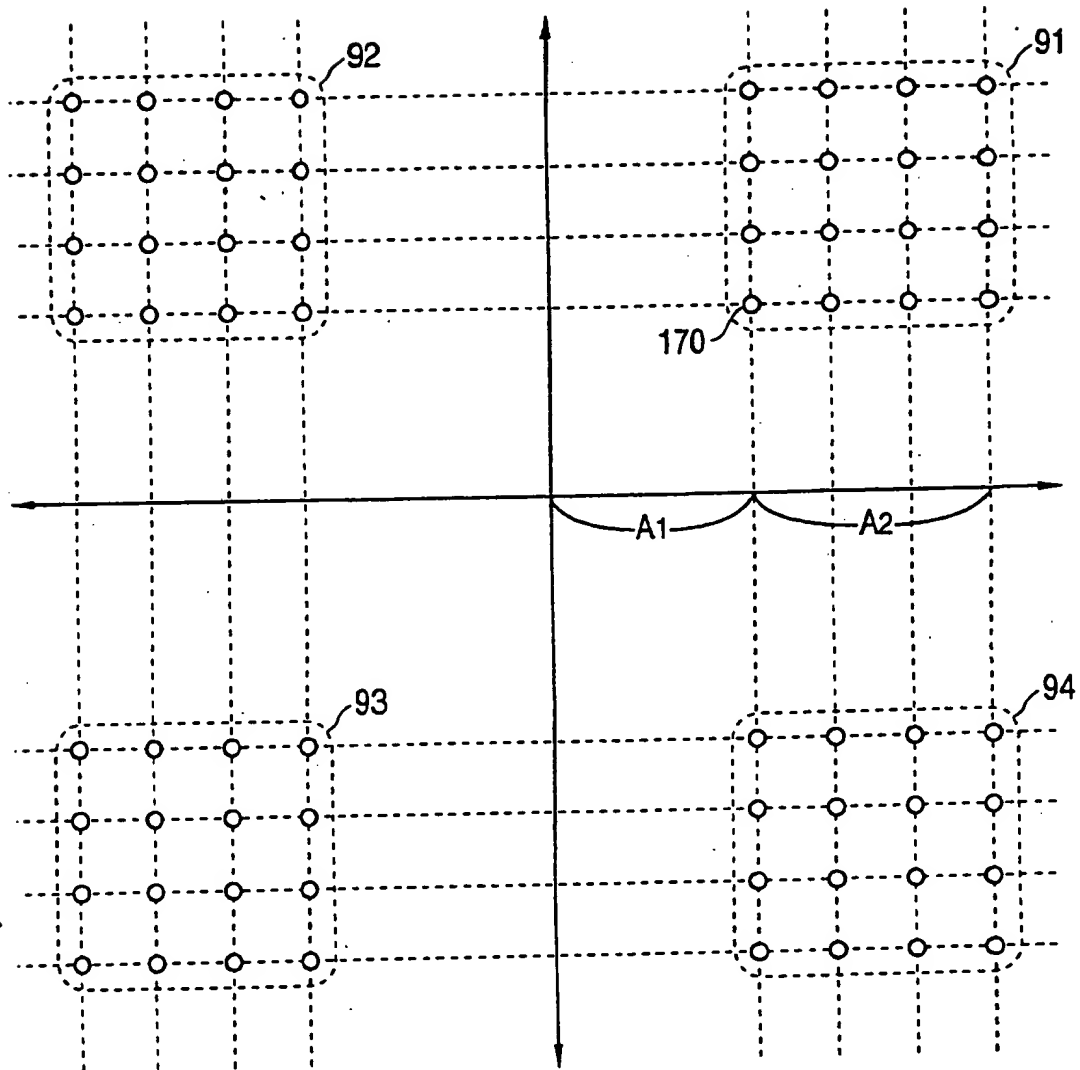


FIG. 12

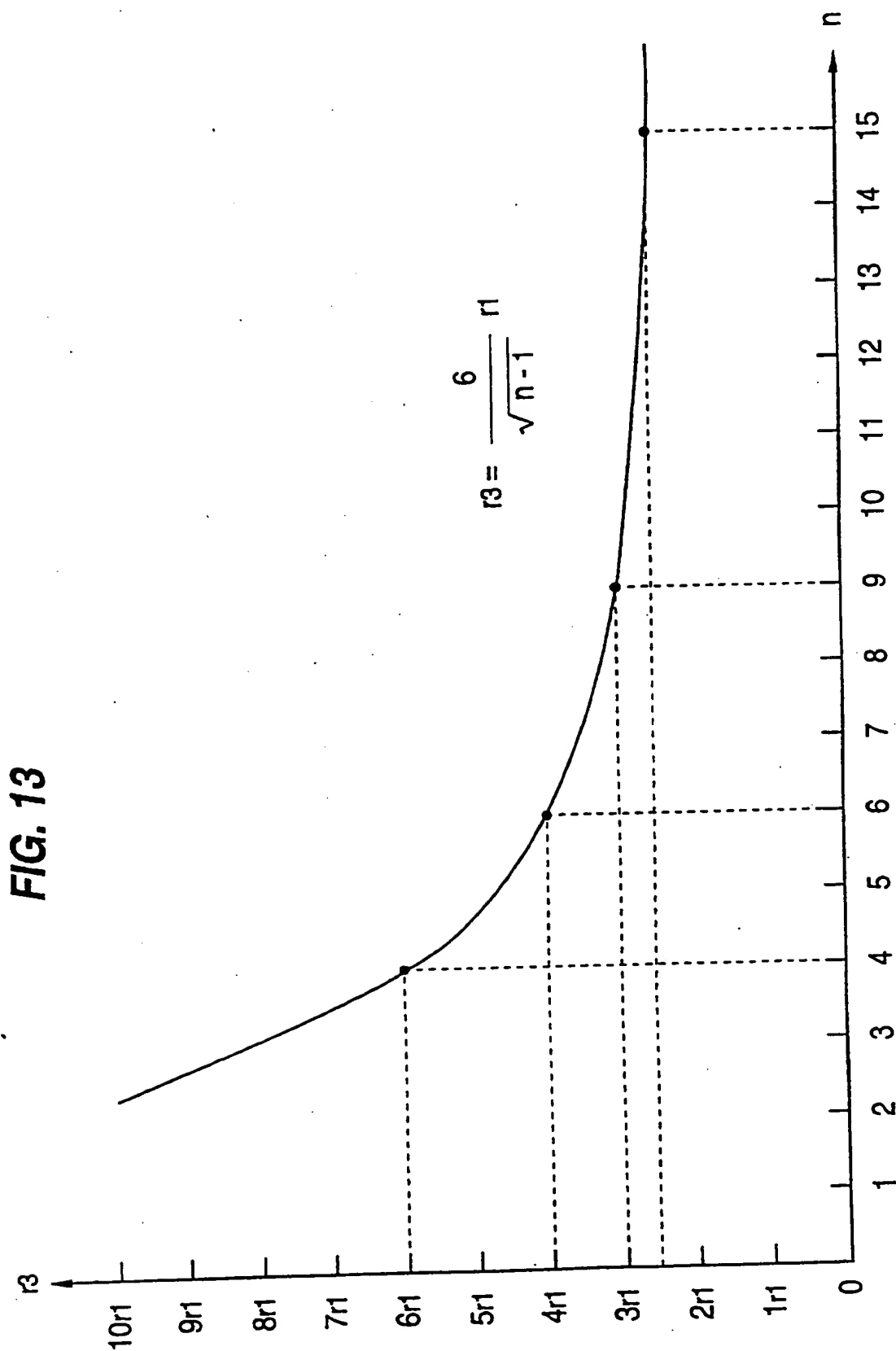


FIG. 14

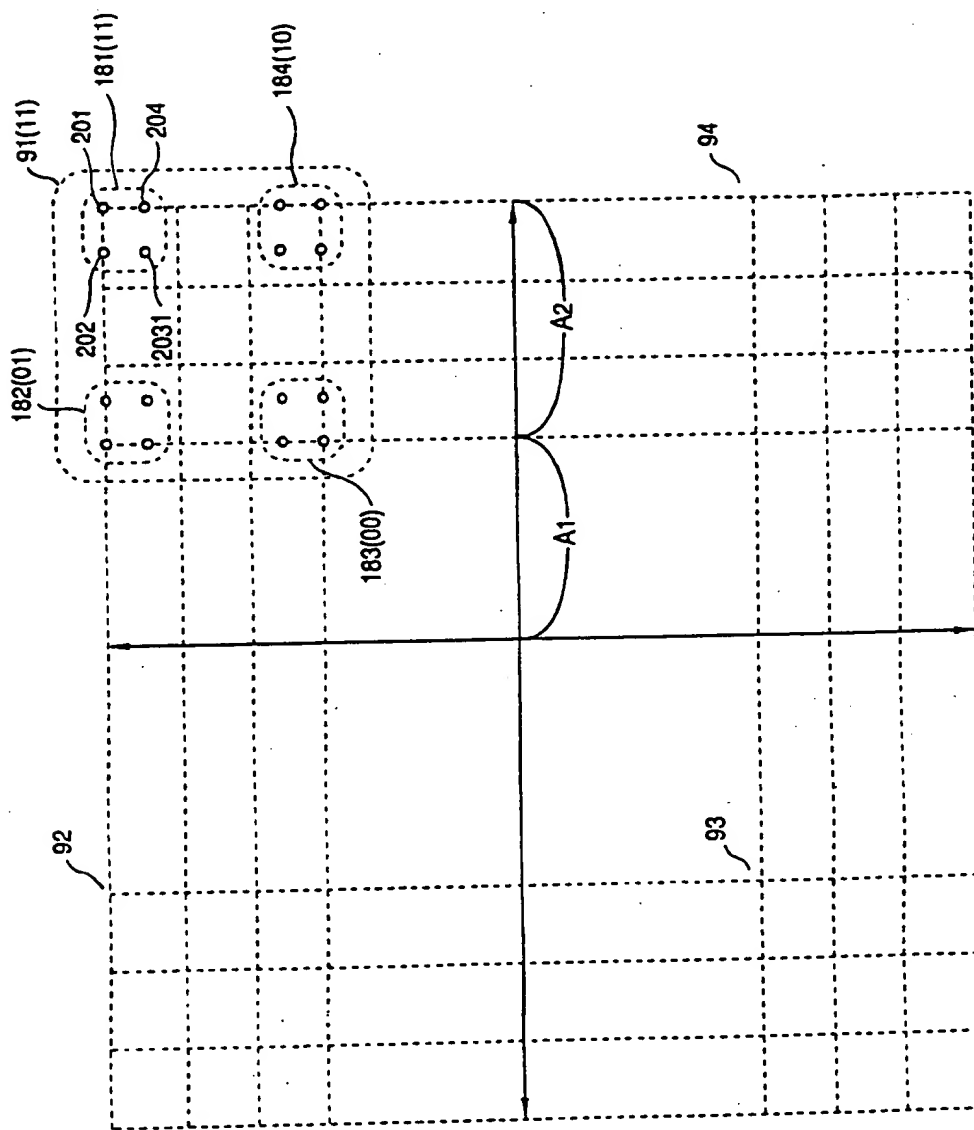


FIG. 15

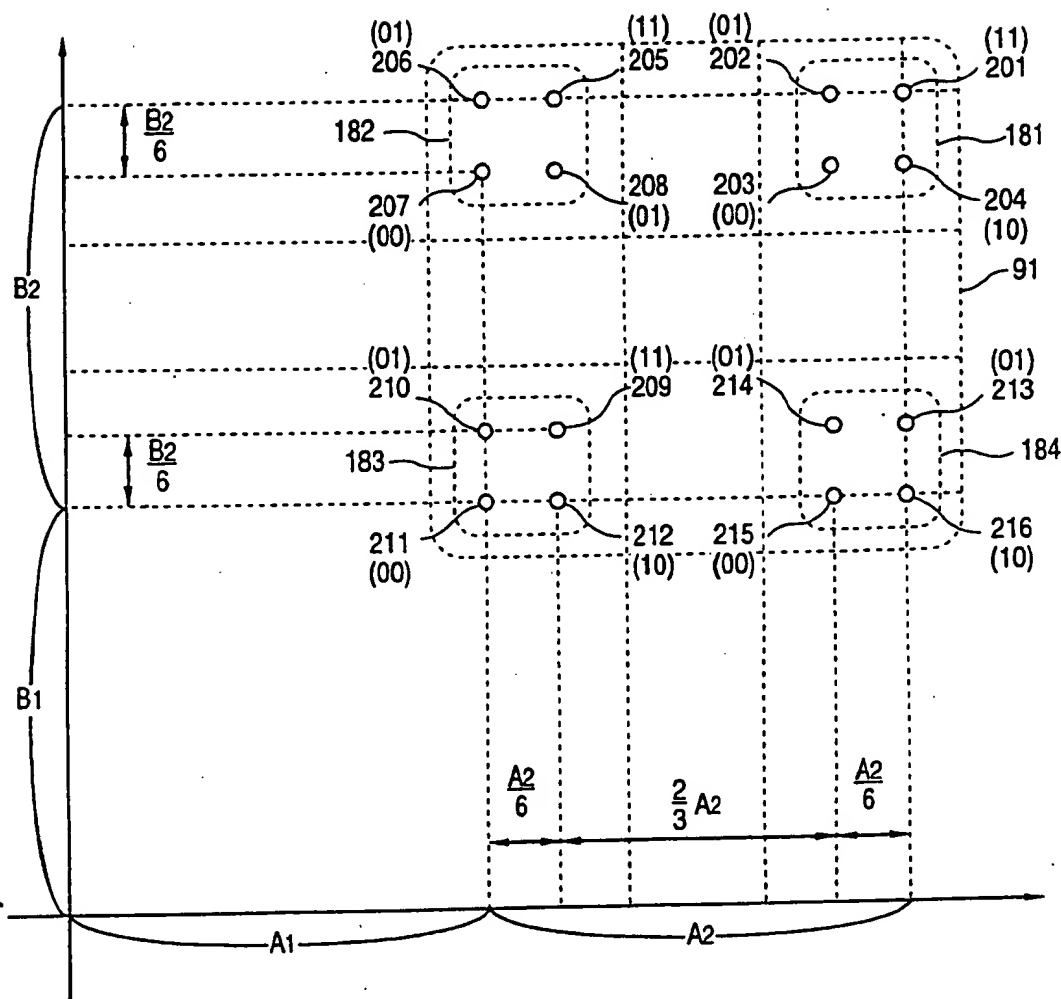


FIG. 16

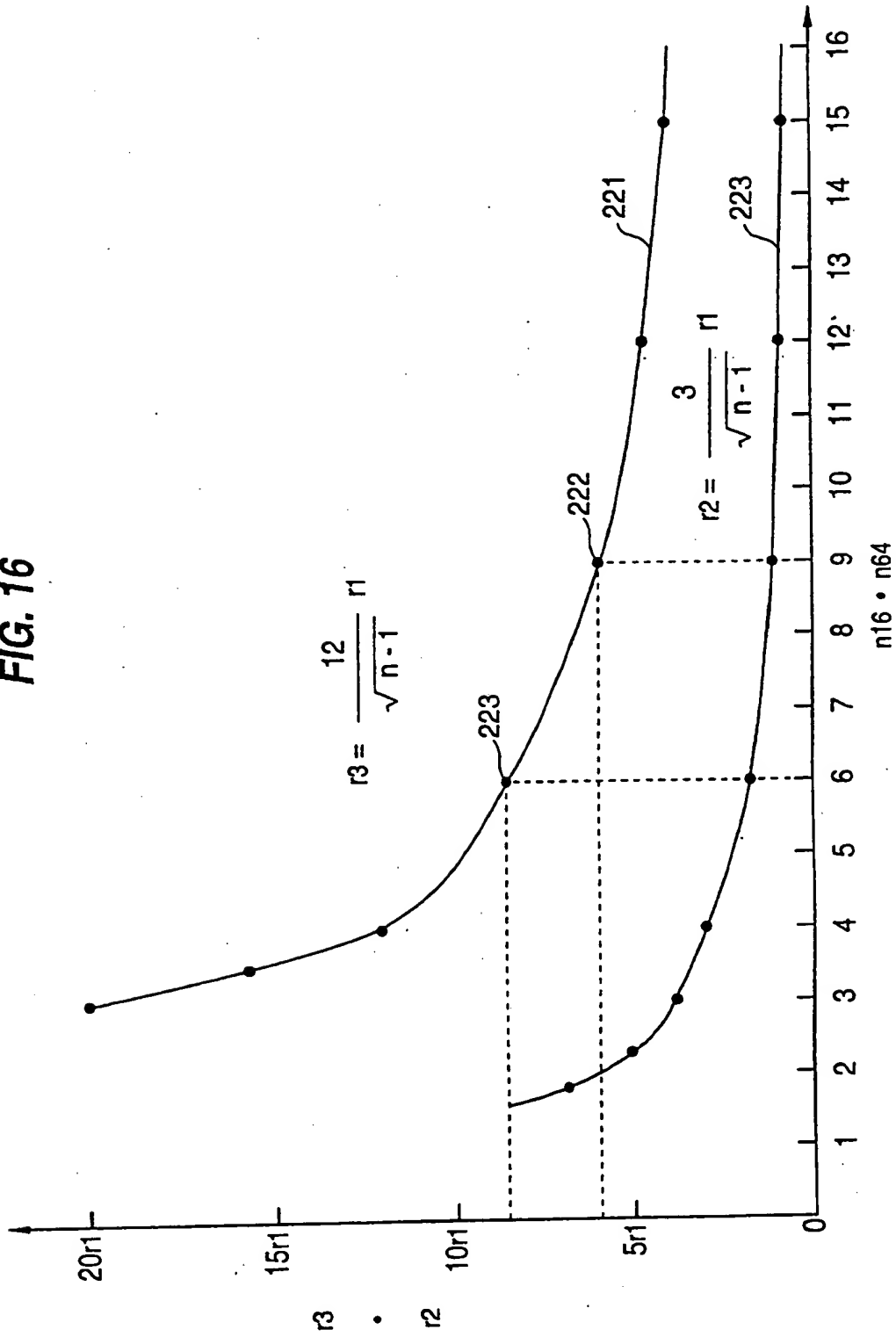


FIG. 17

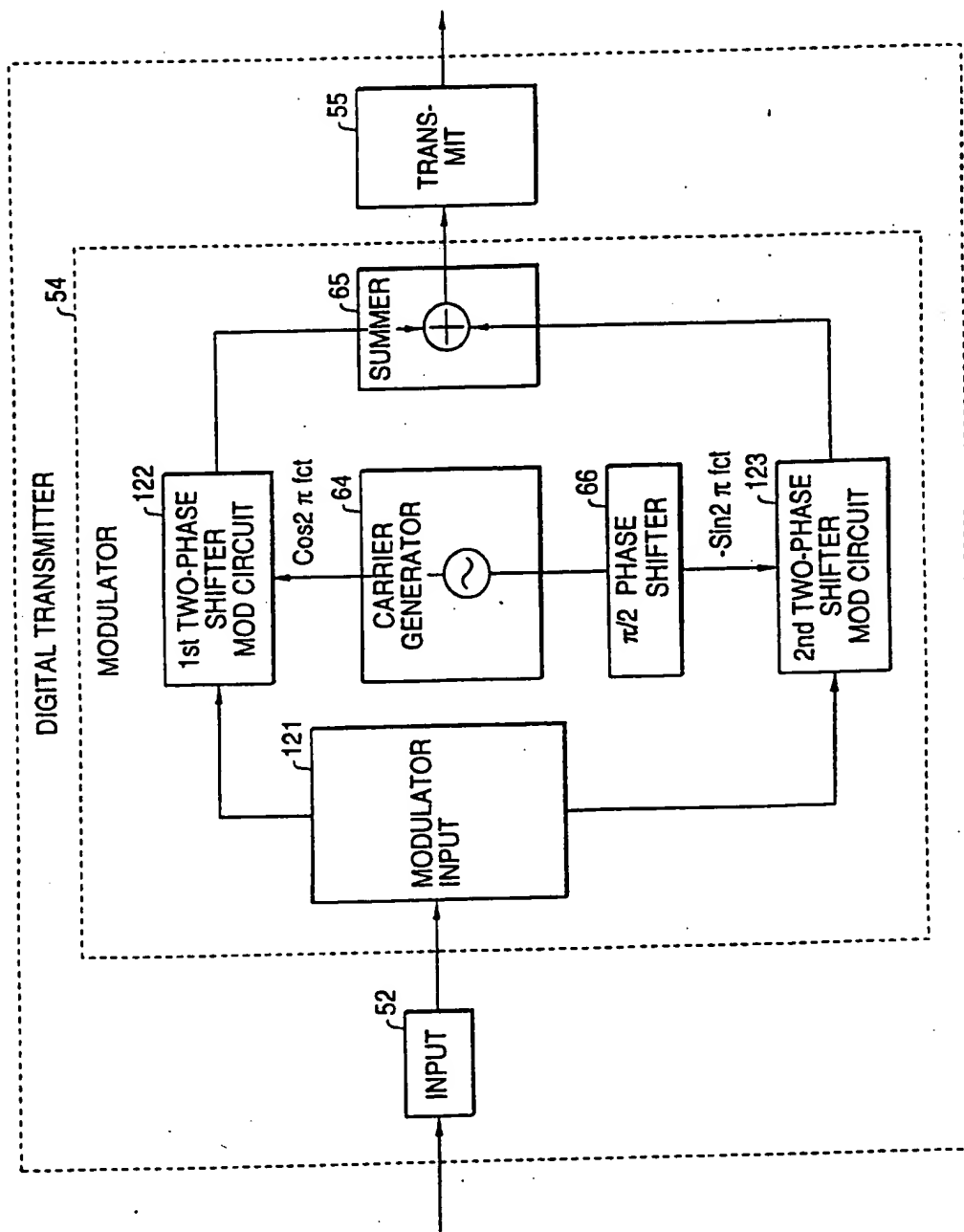
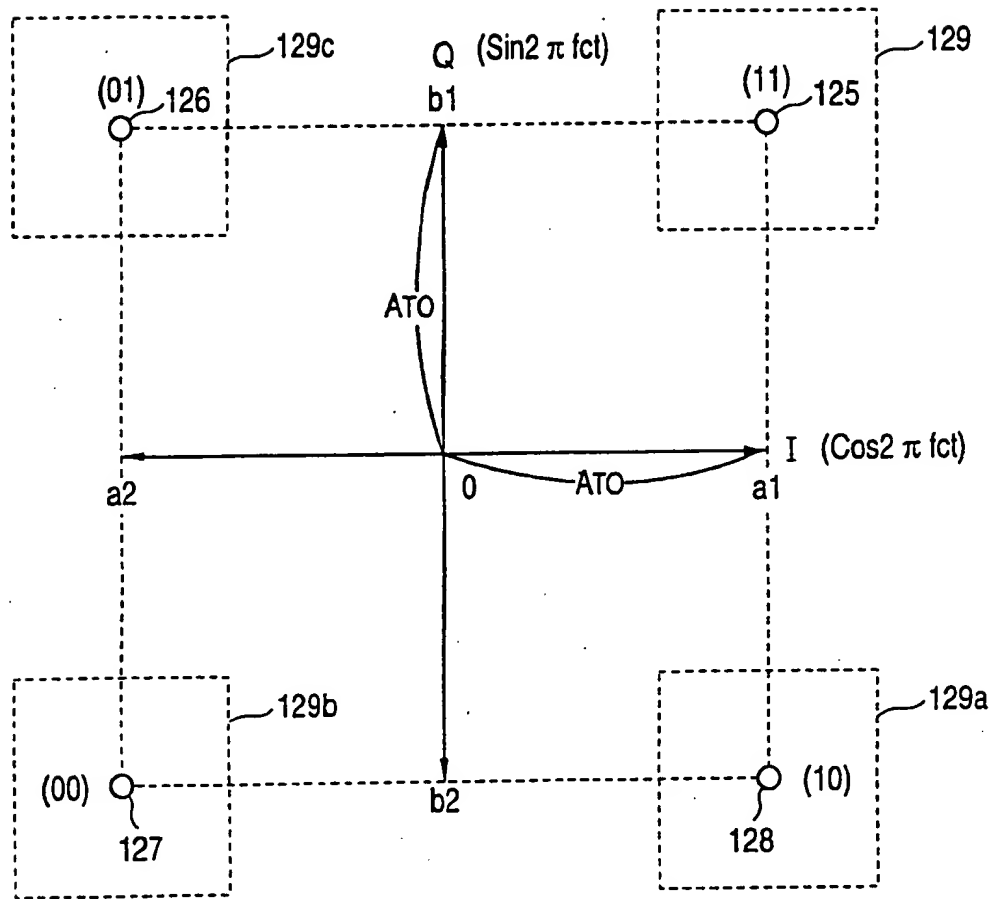


FIG. 18



005017-100500

FIG. 19

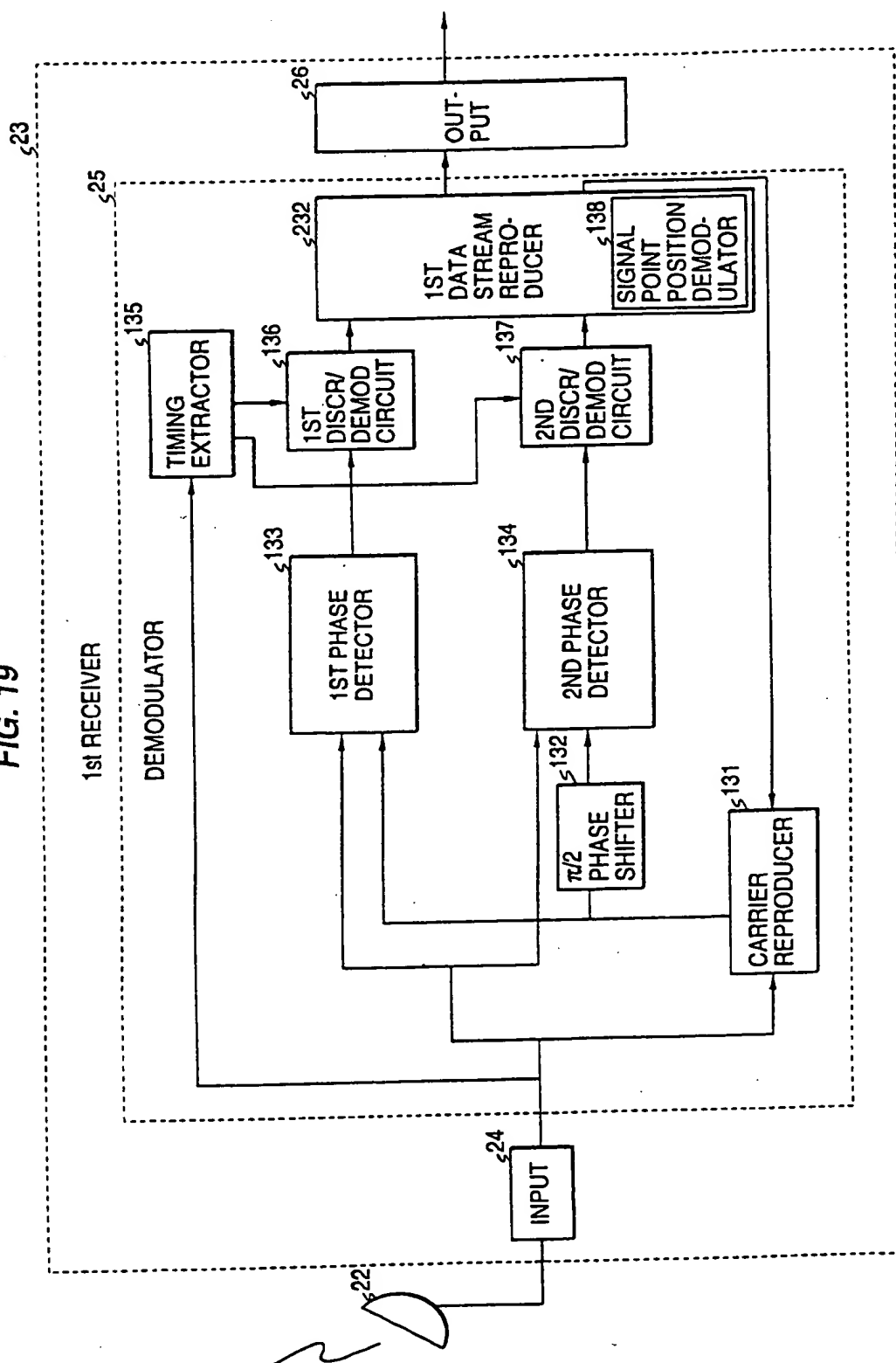
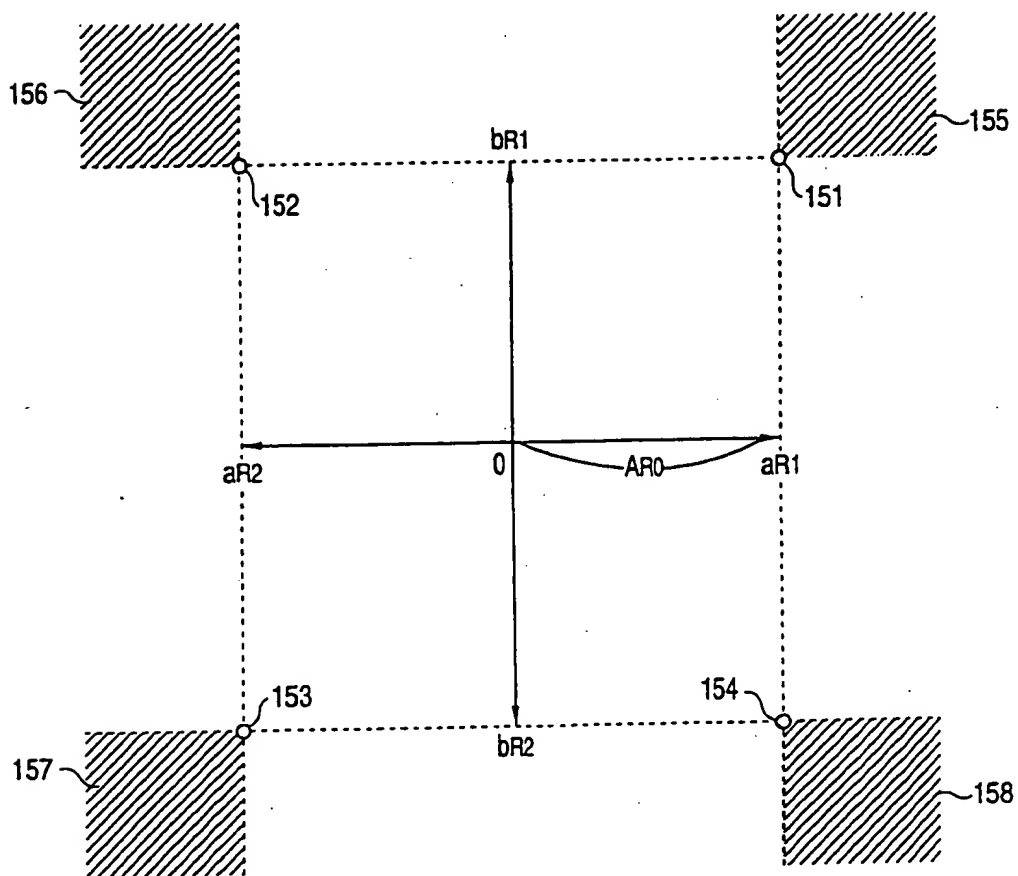


FIG. 20



000001-1000

FIG. 21

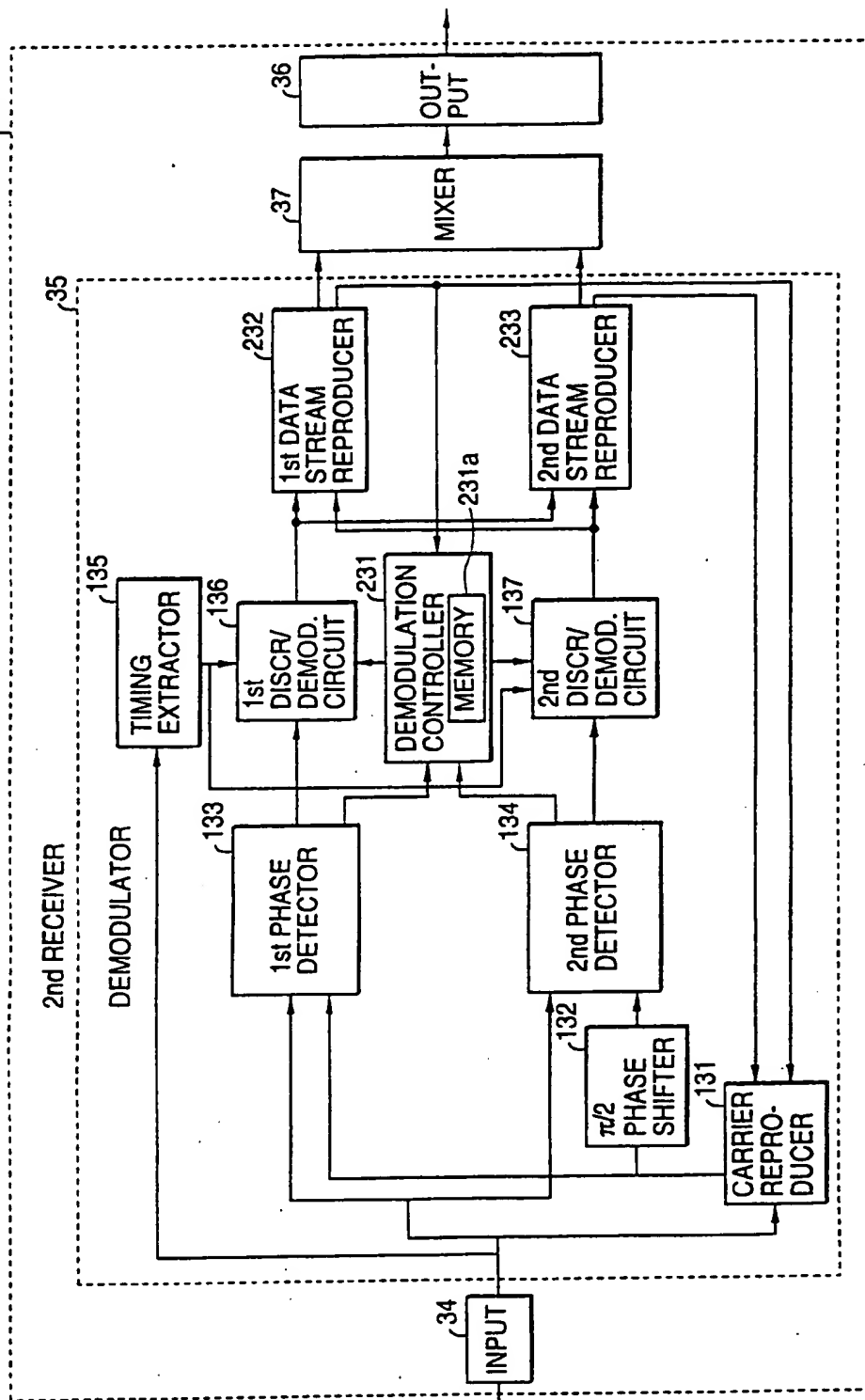


FIG. 22

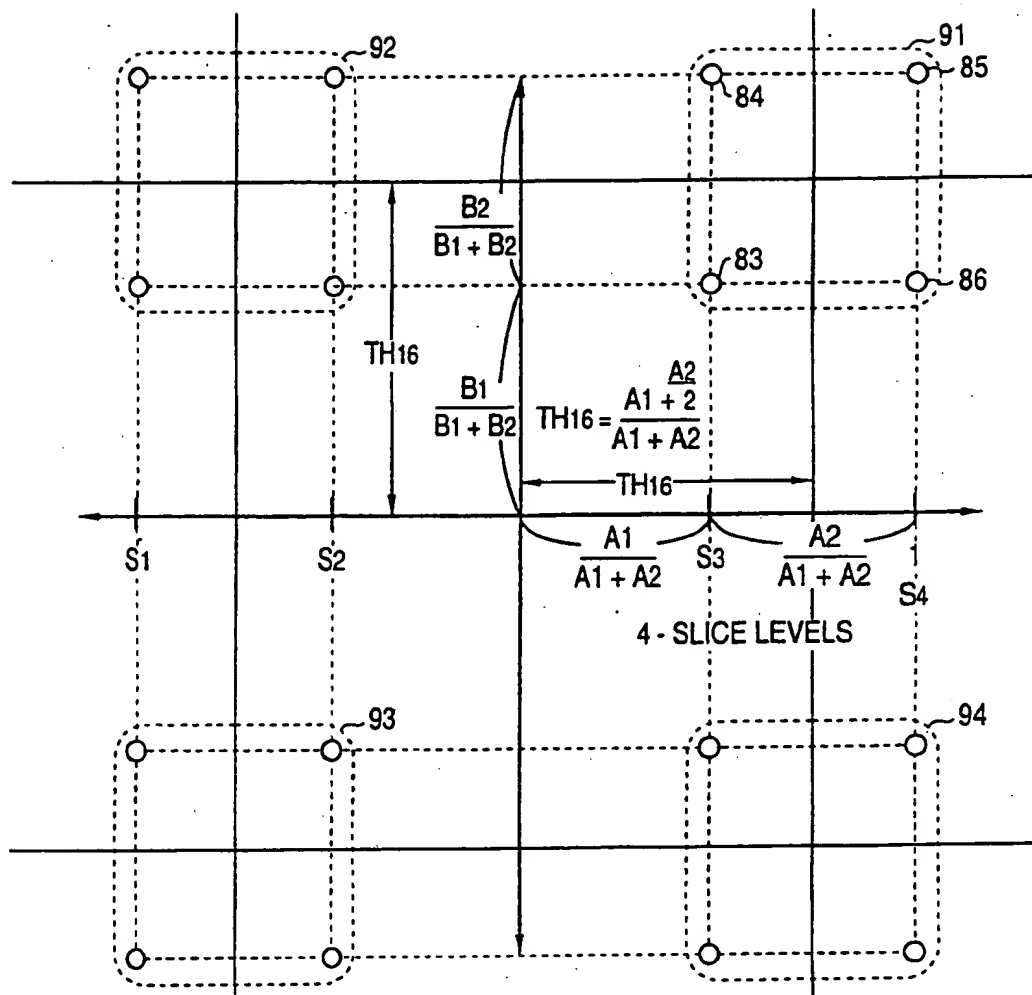
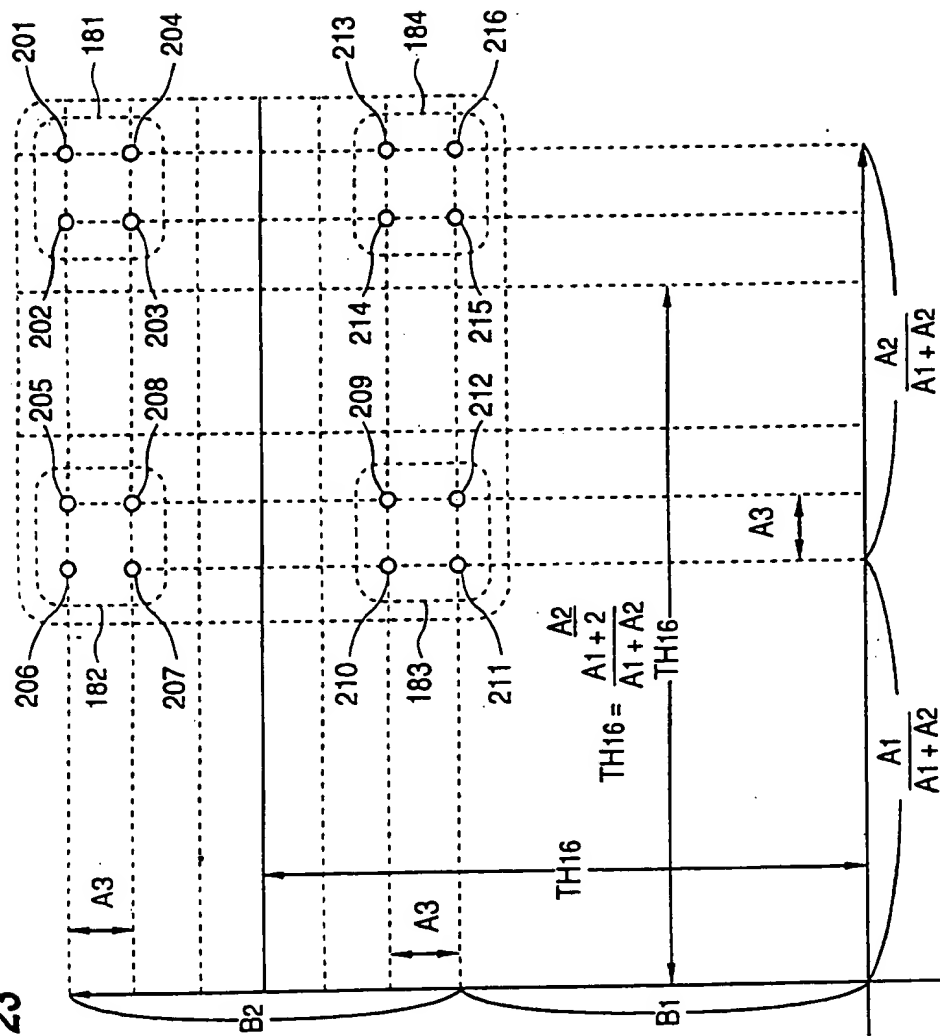


FIG. 23



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FIG. 24

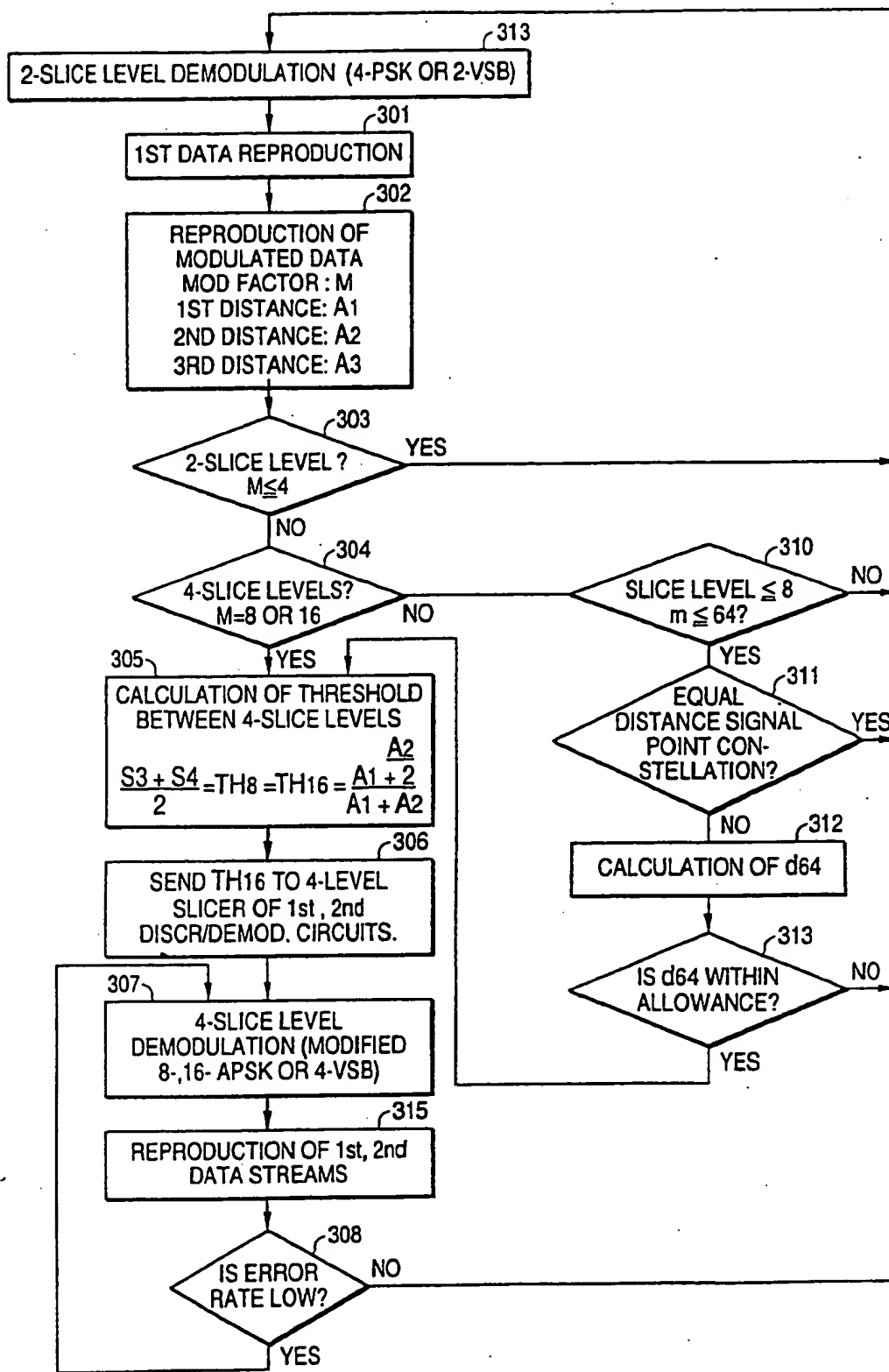


FIG. 25(a)

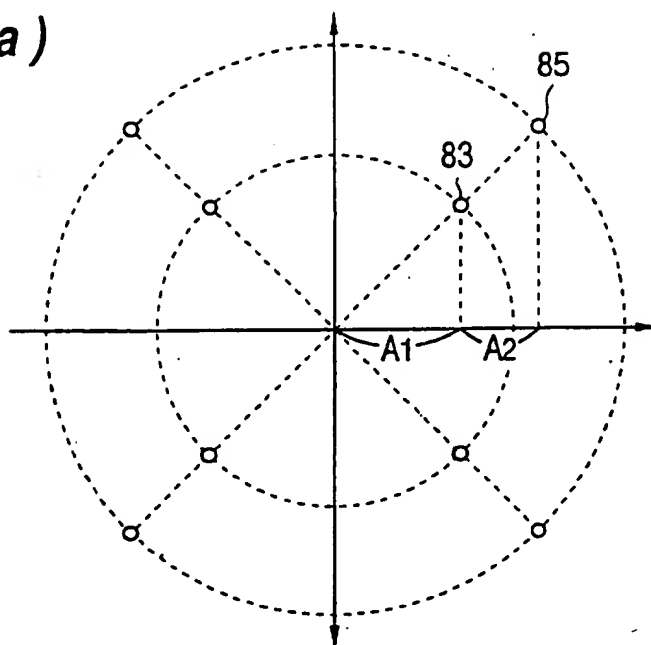
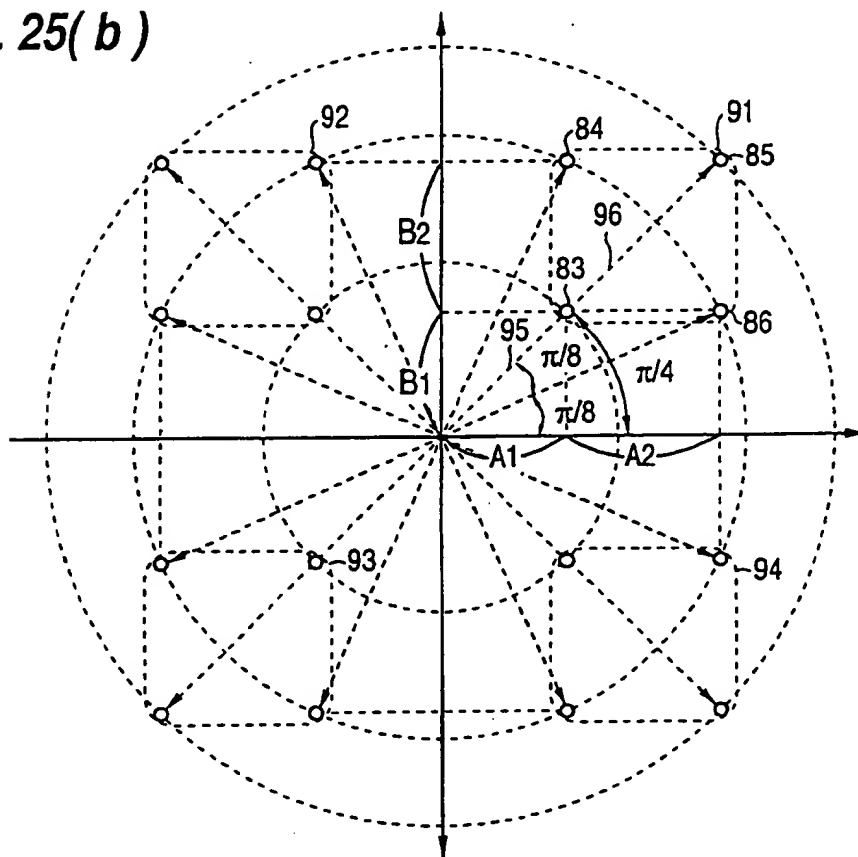
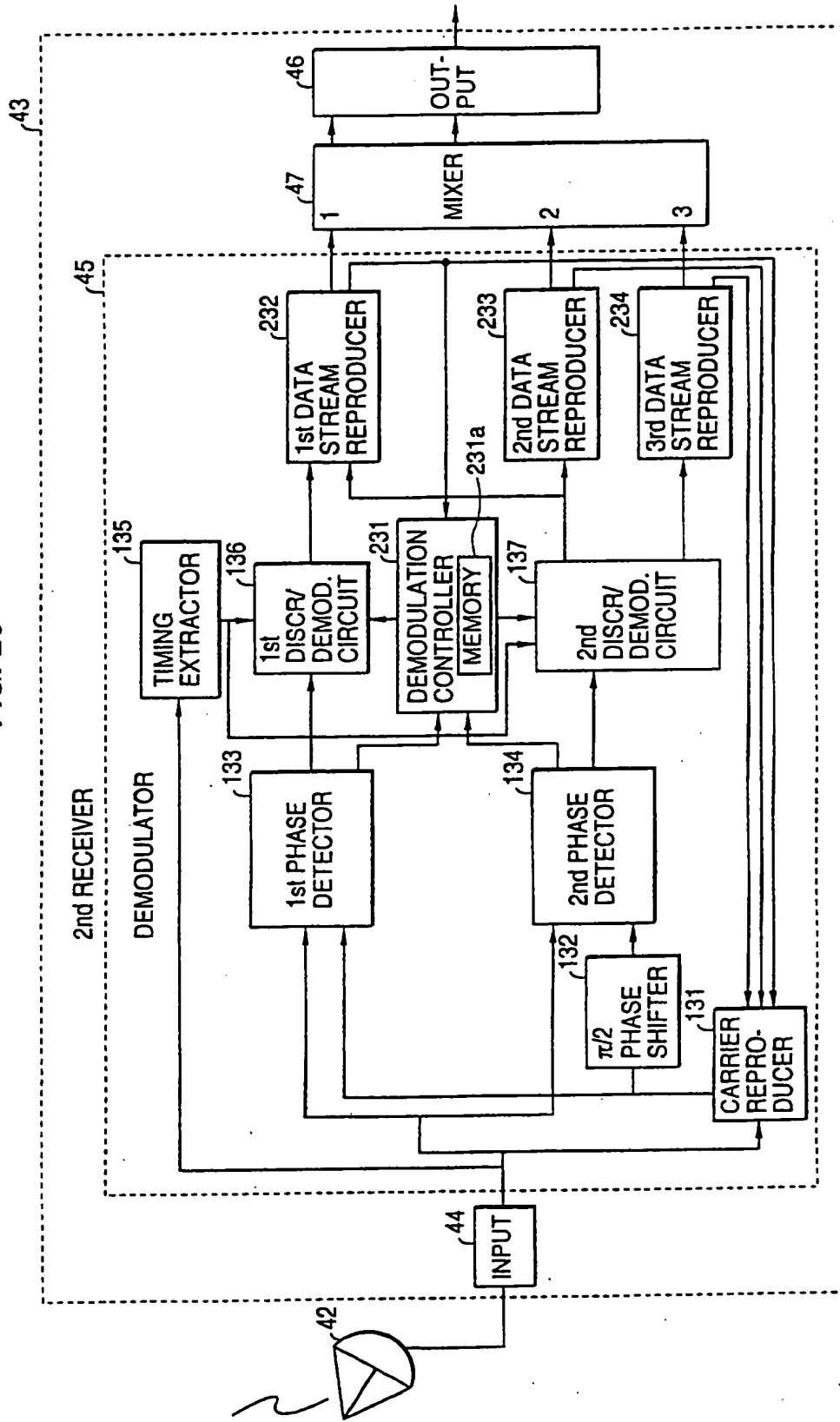


FIG. 25(b)



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FIG. 26



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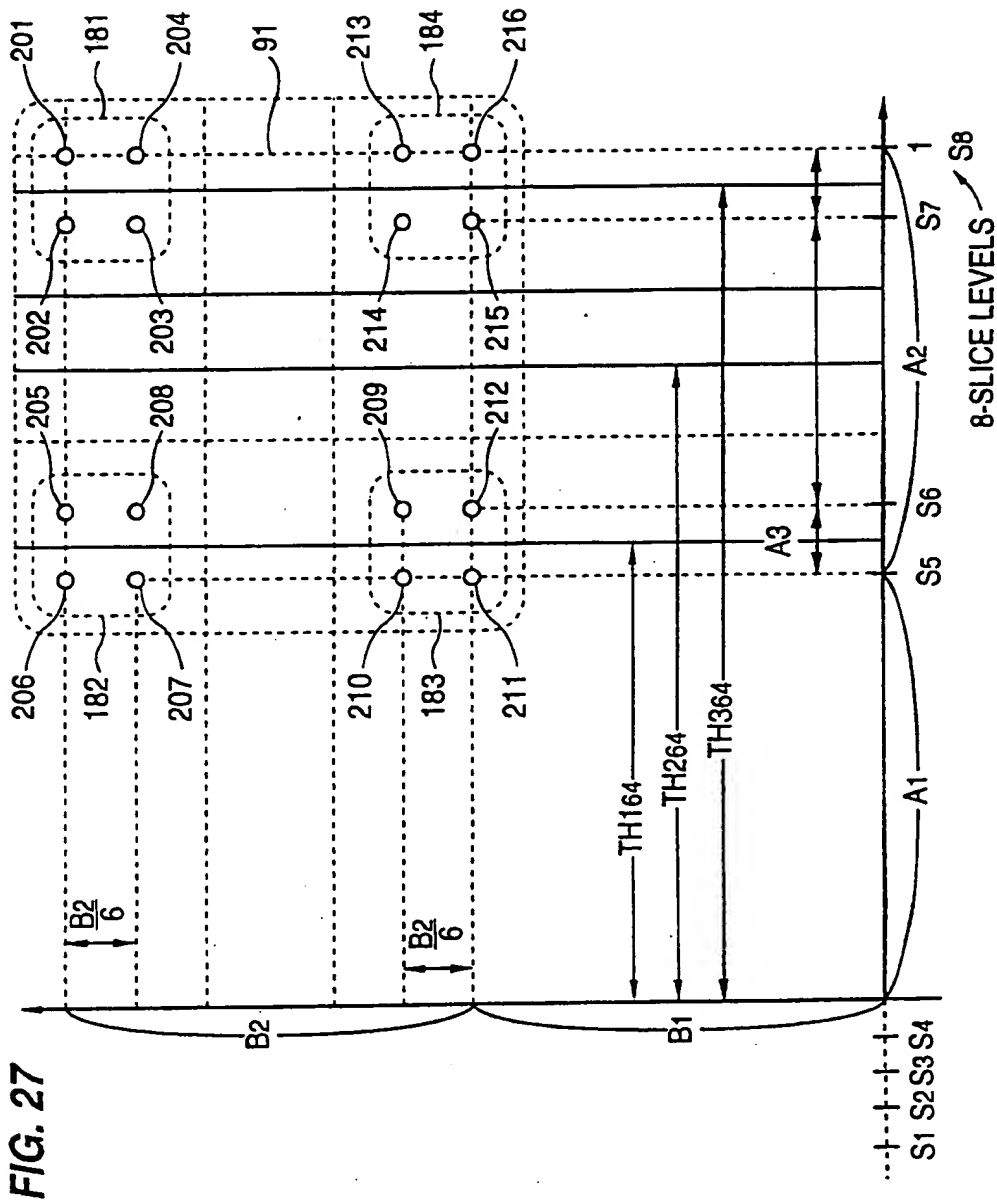


FIG. 28

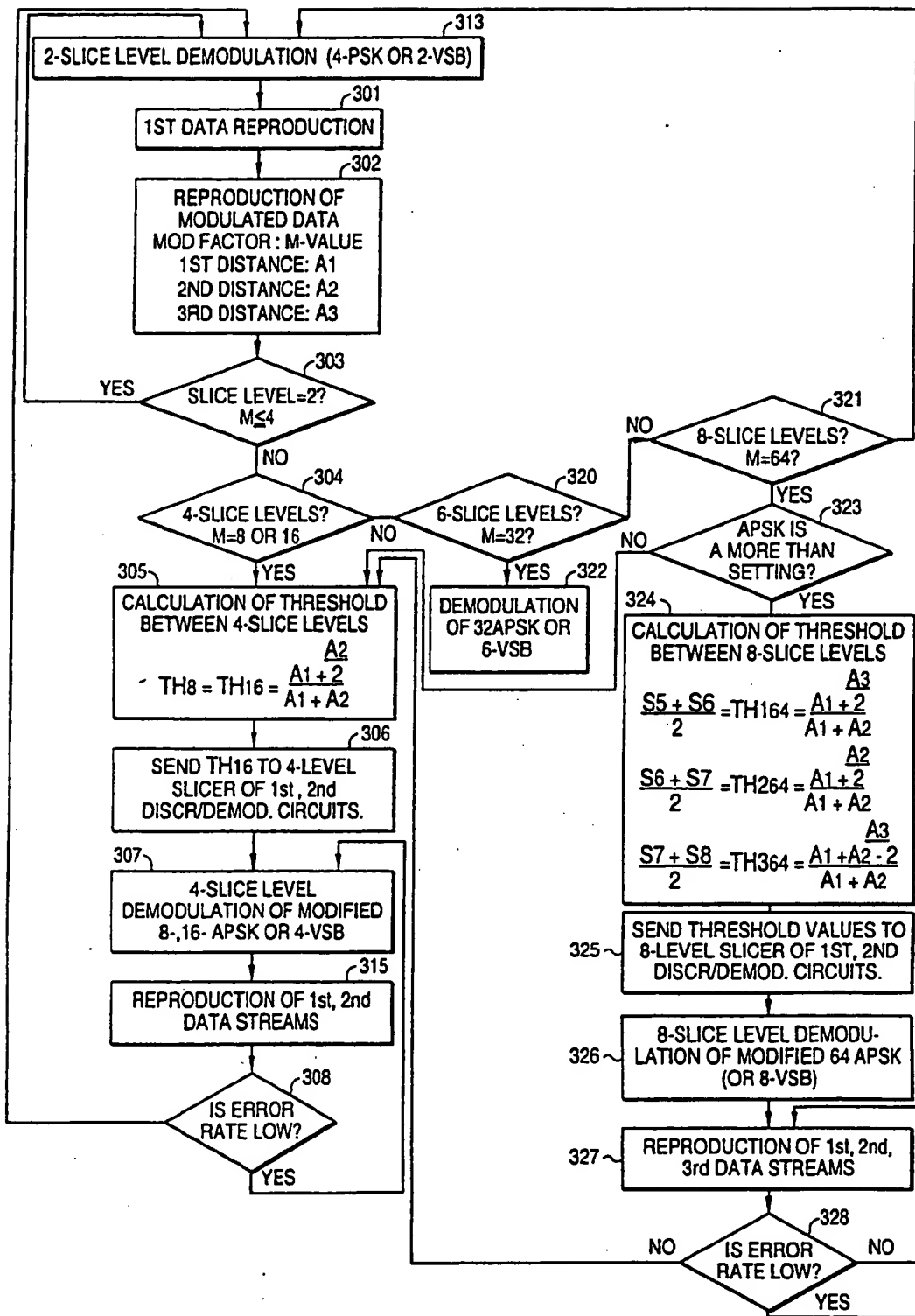


FIG. 29

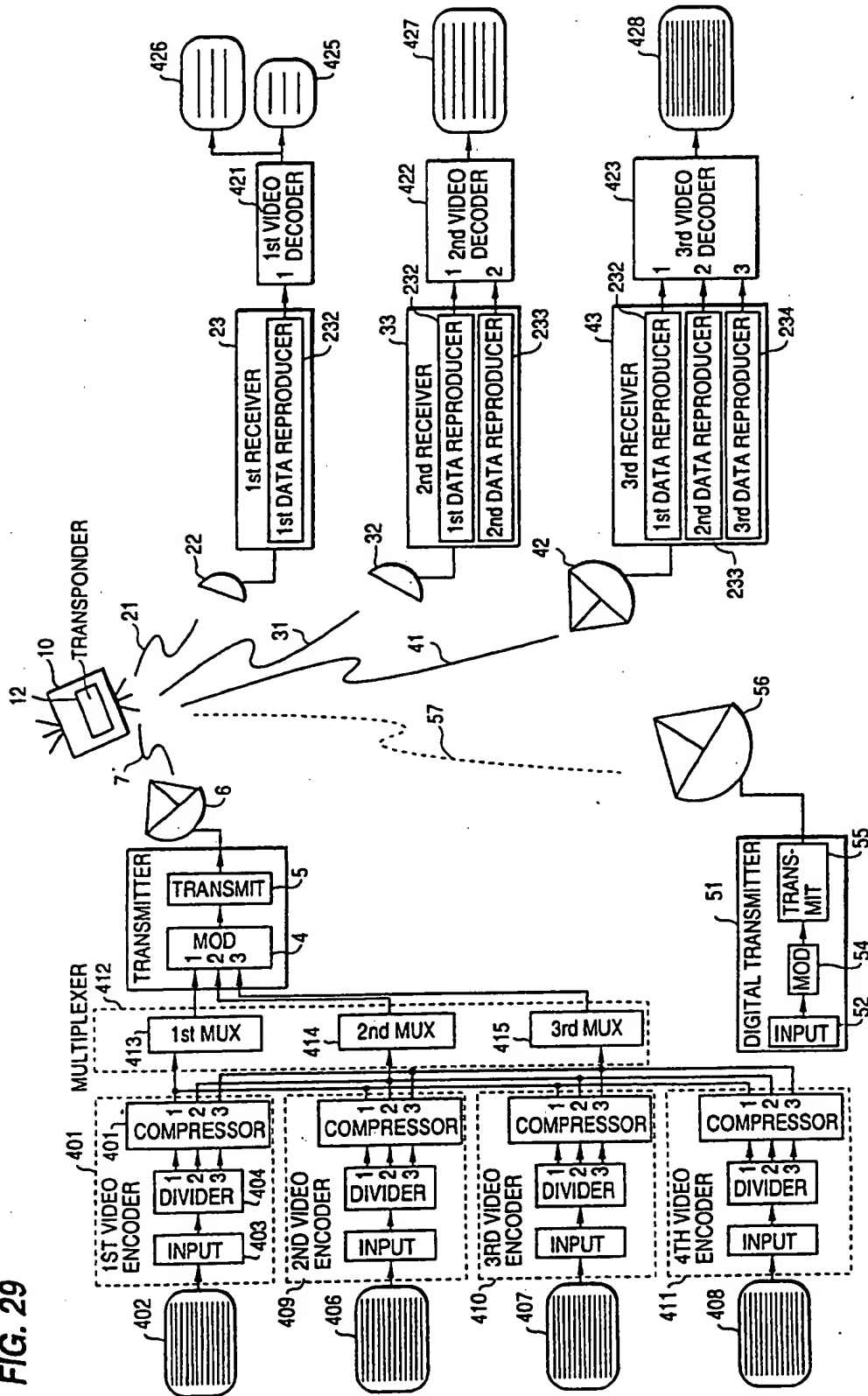
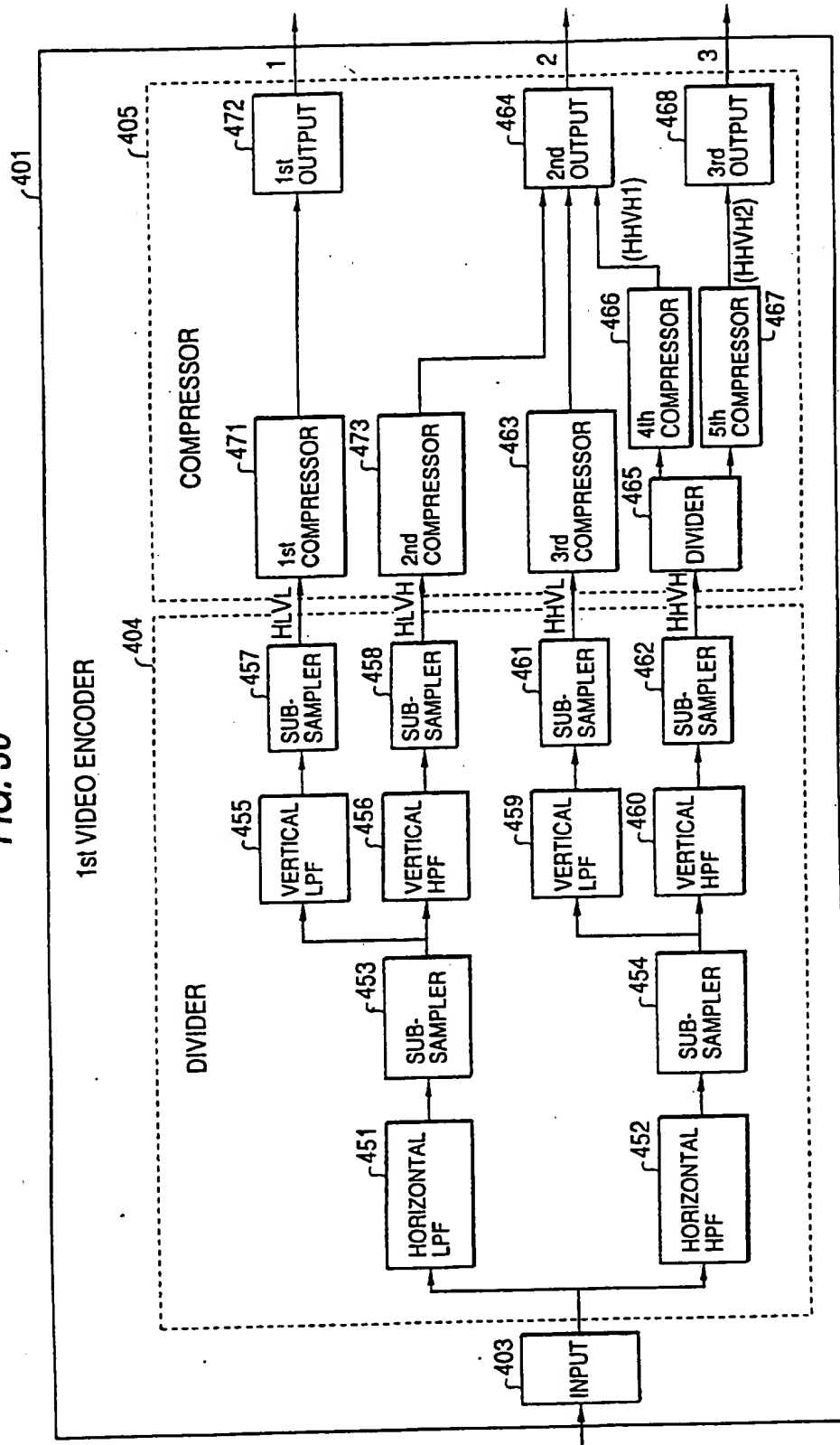
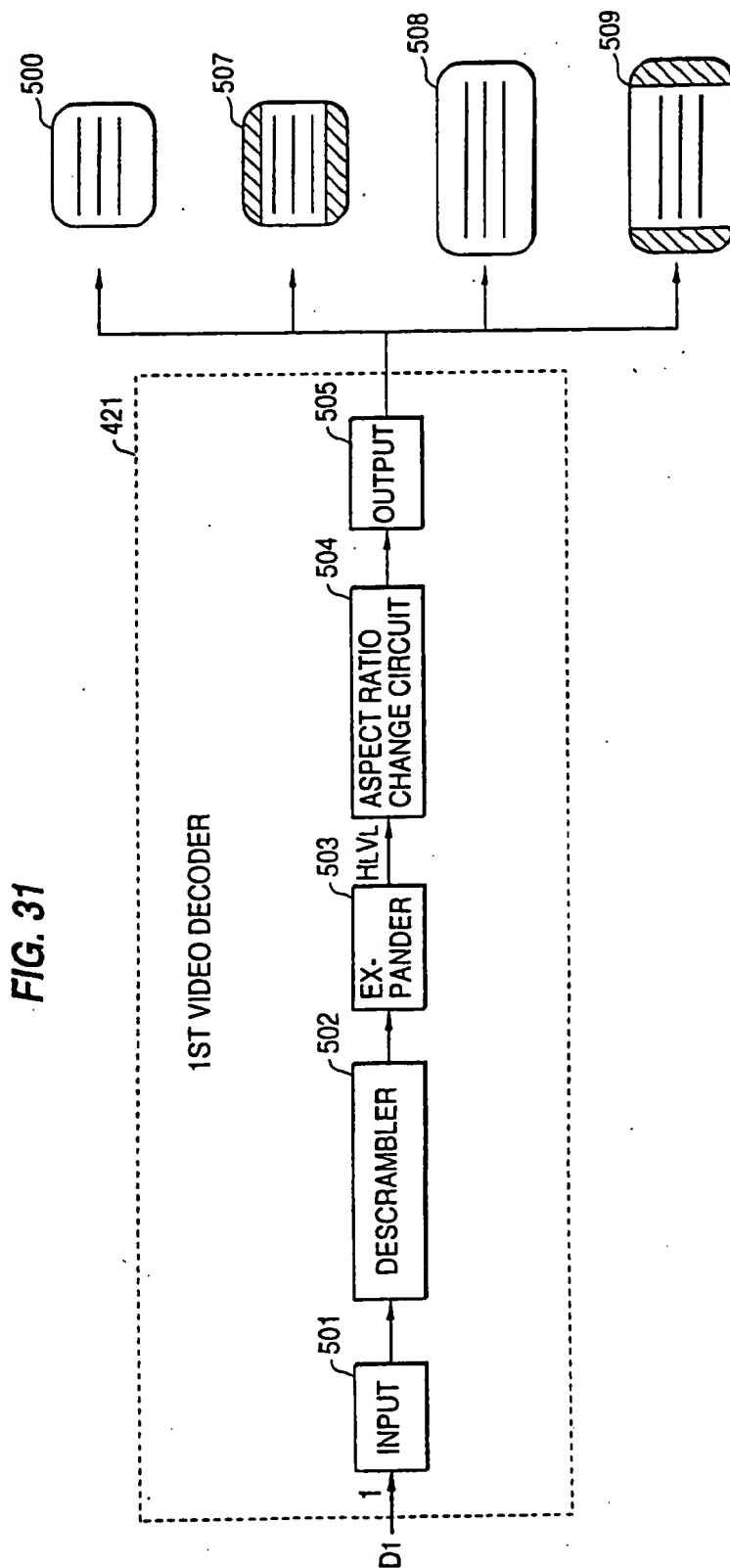


FIG. 30





00500T" 2209360

FIG. 32

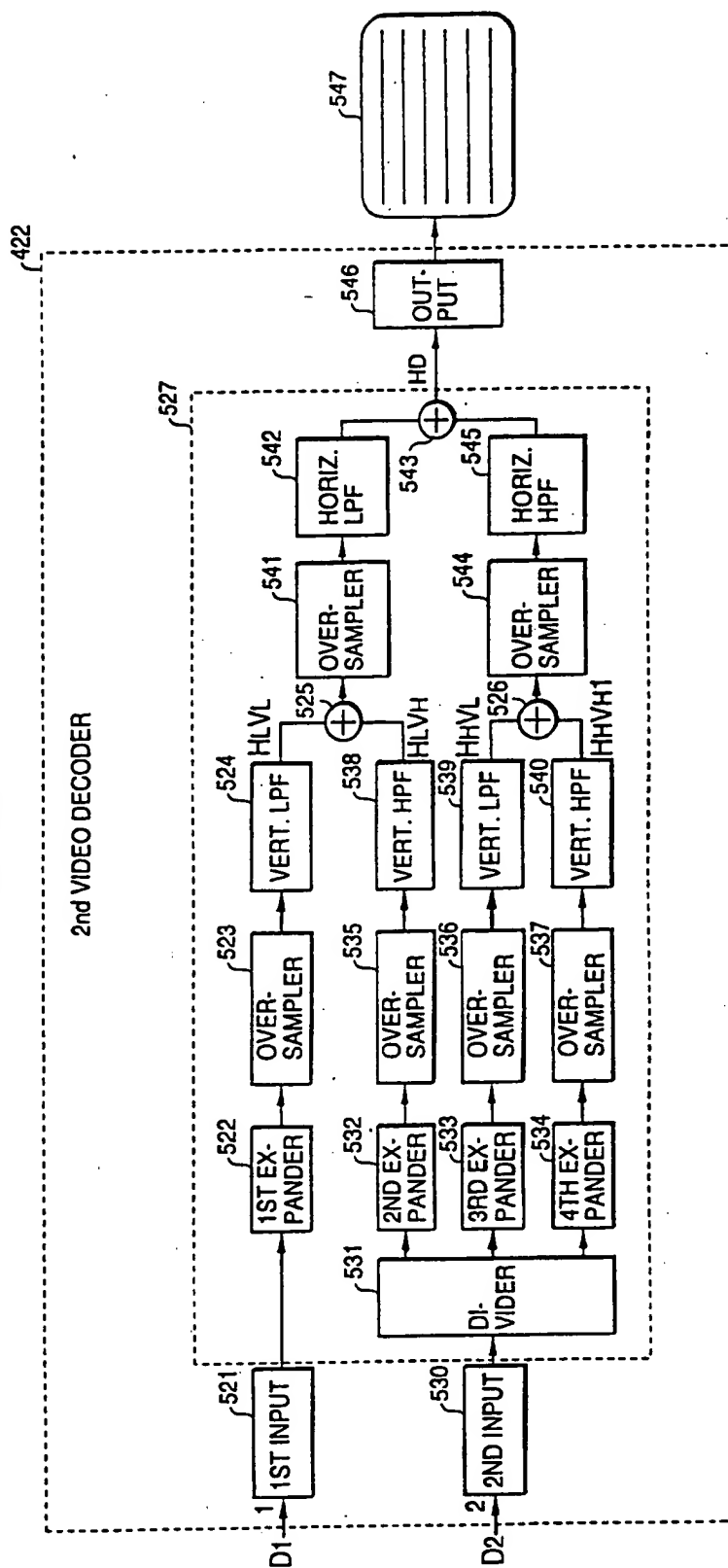


FIG. 33

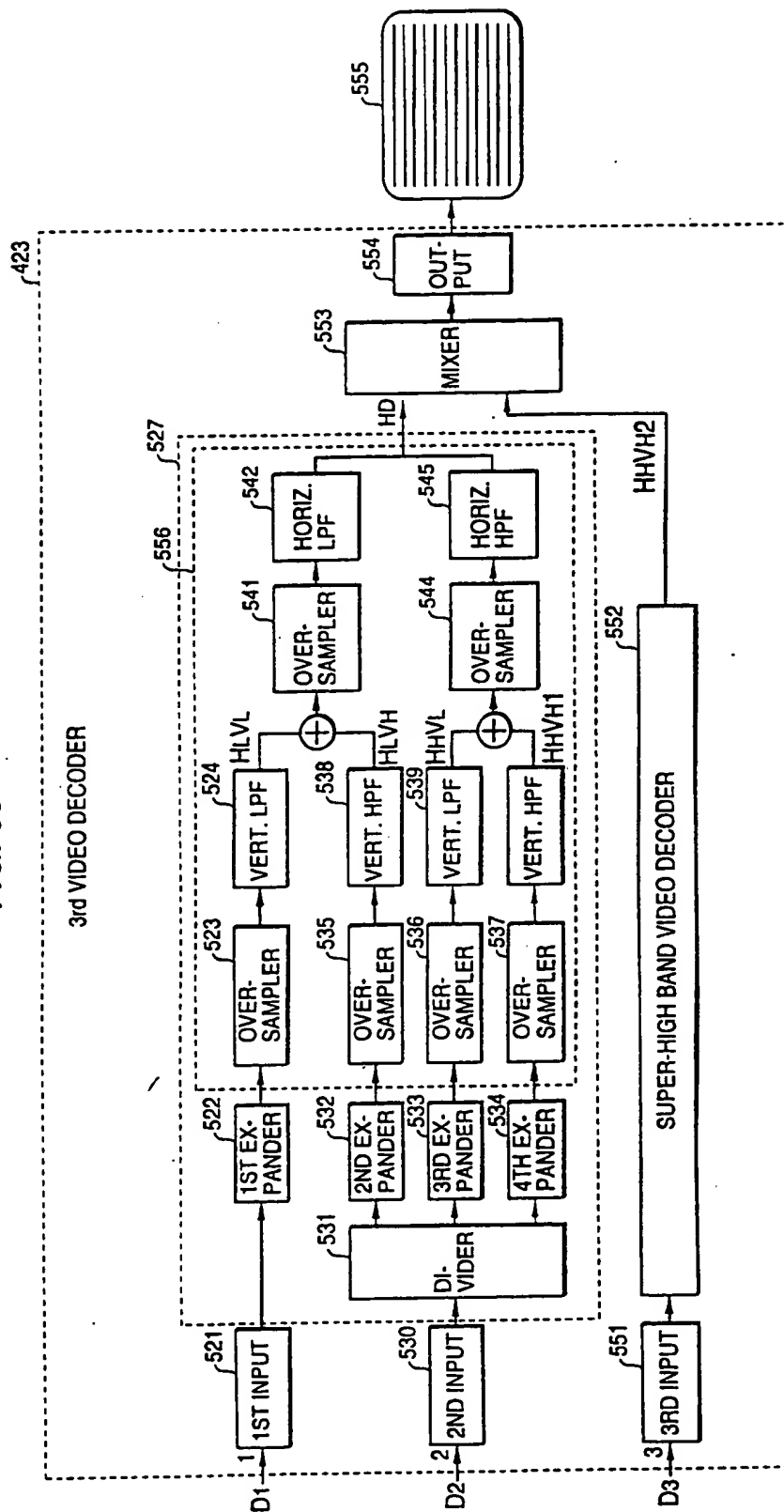


FIG. 34

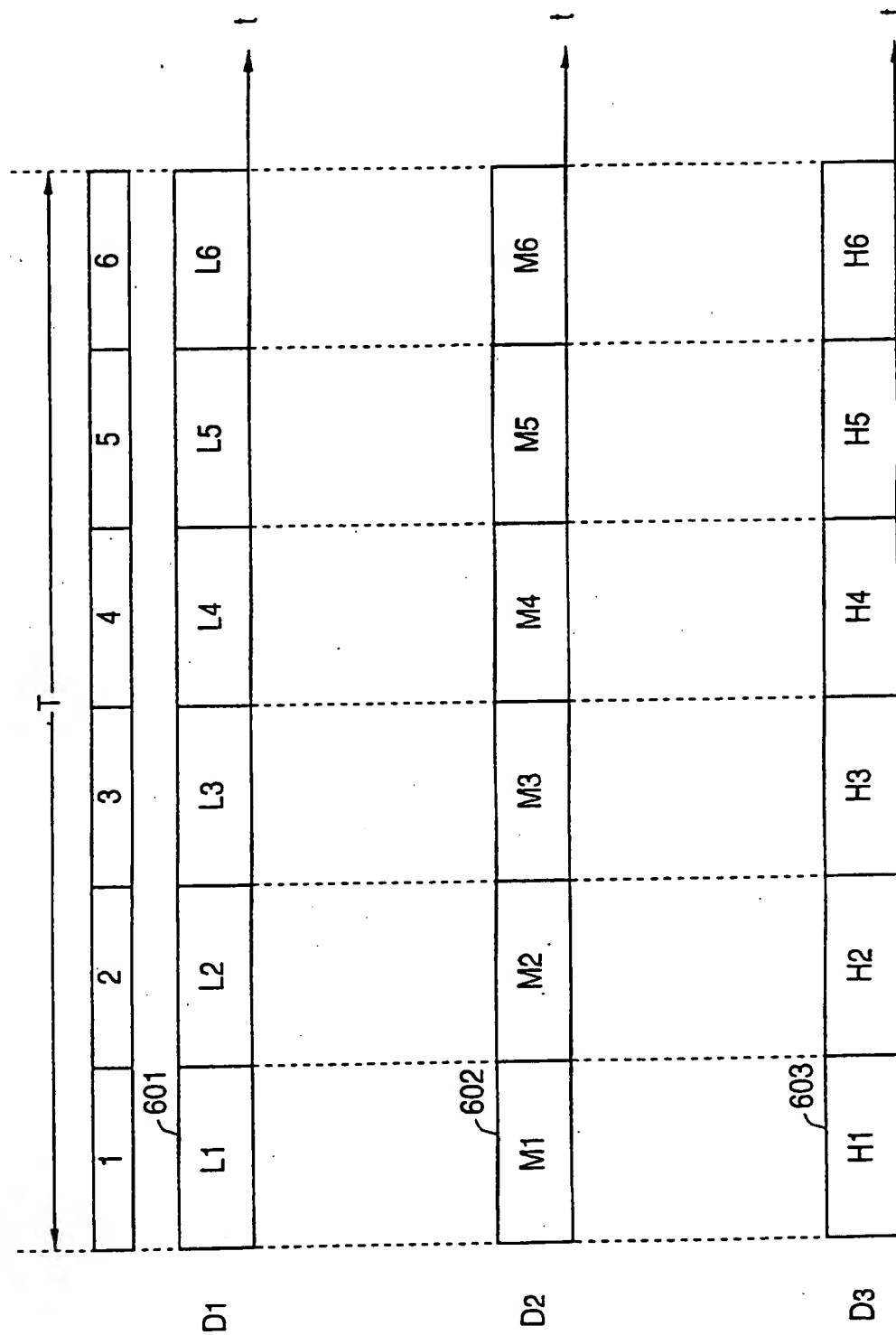


FIG. 35

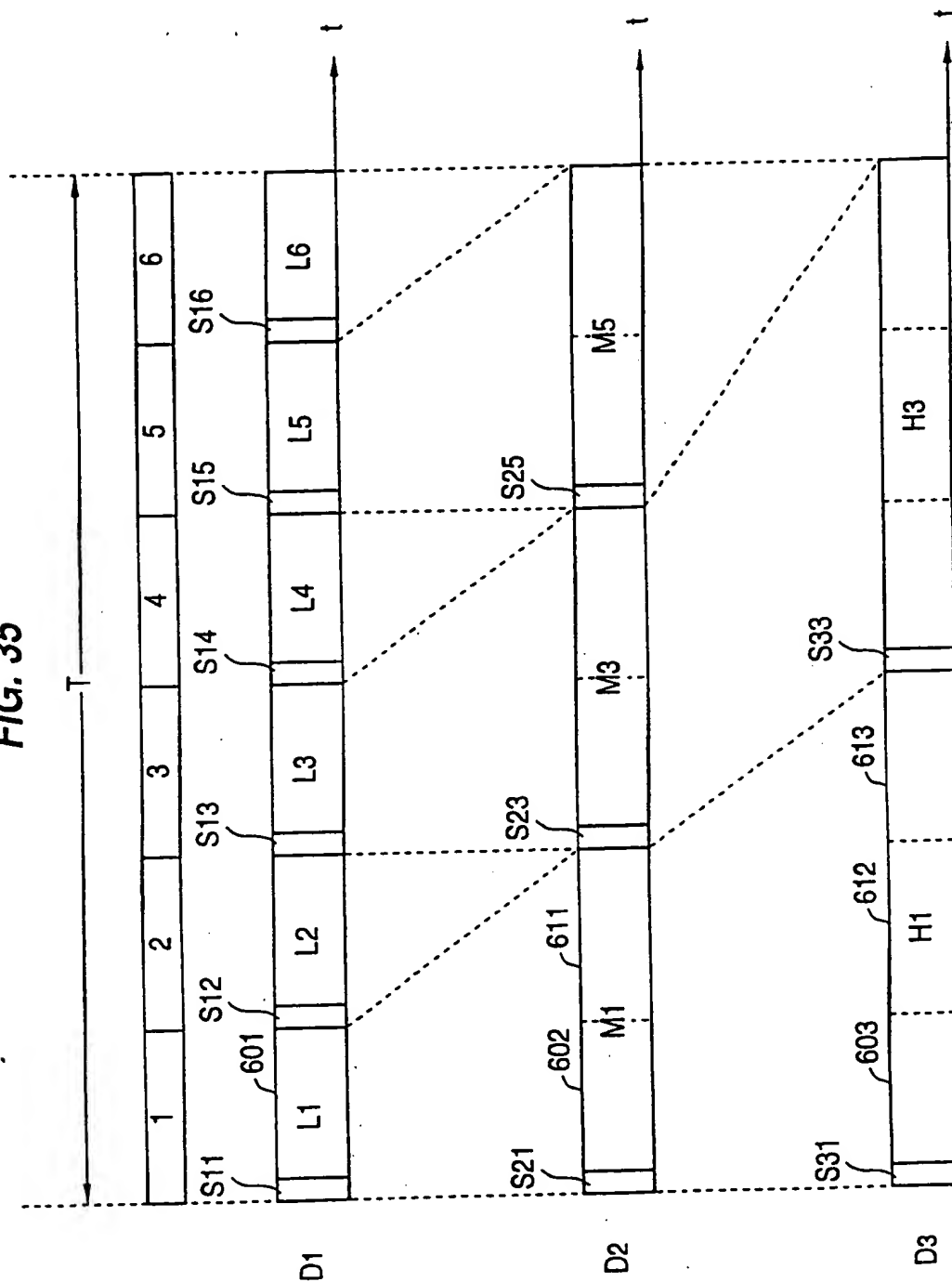


FIG. 36

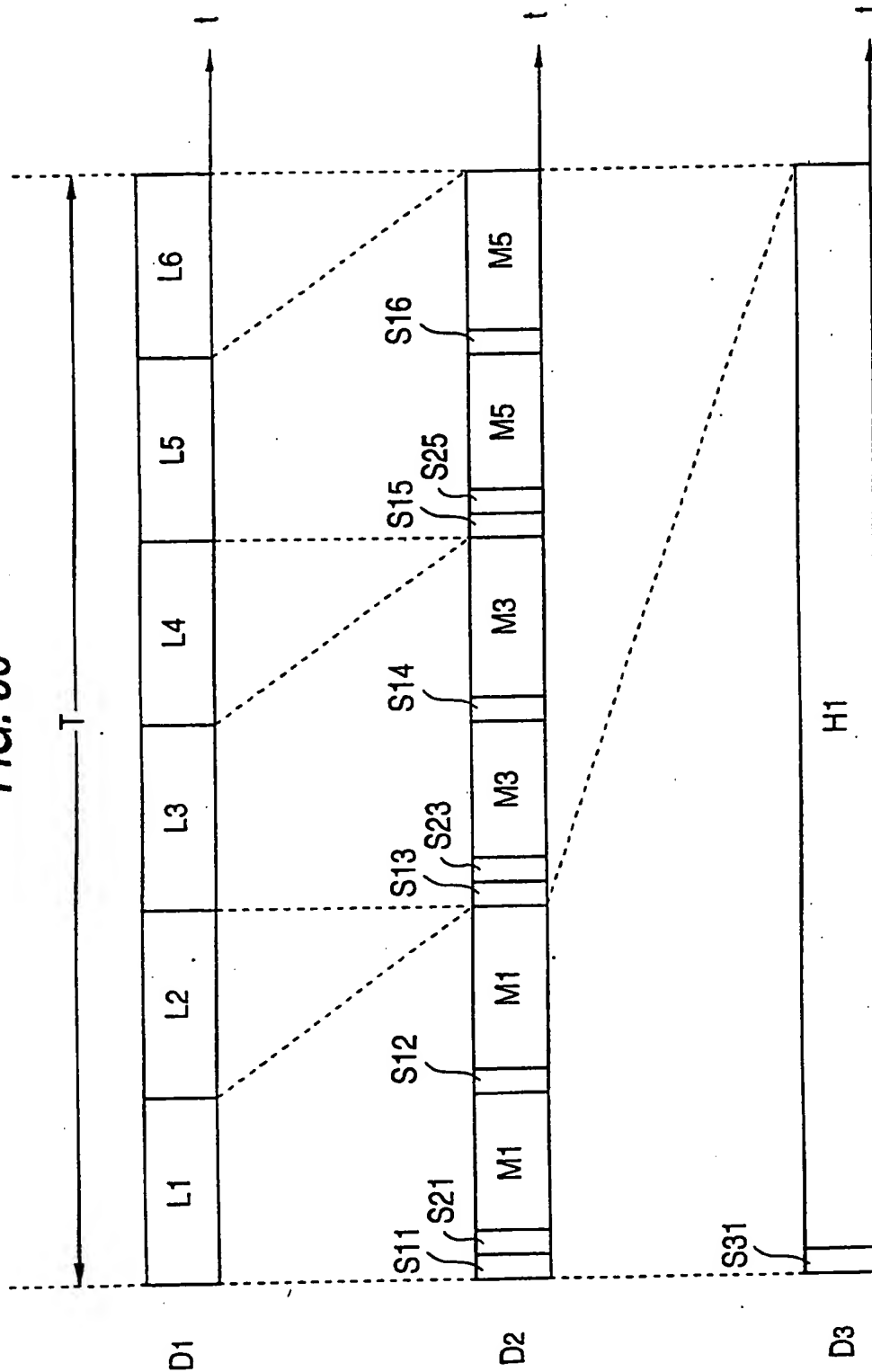


FIG. 37

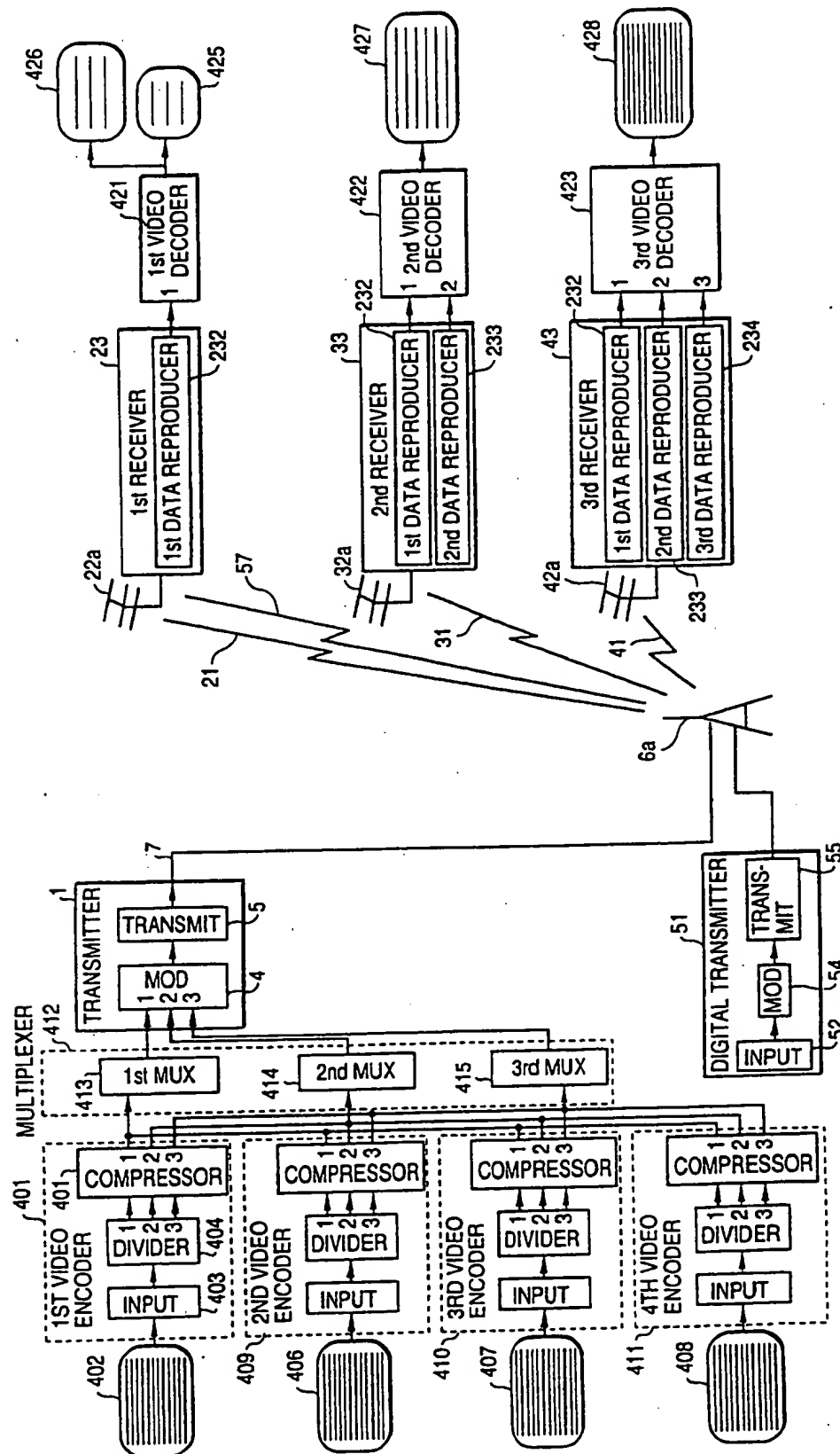


FIG. 38

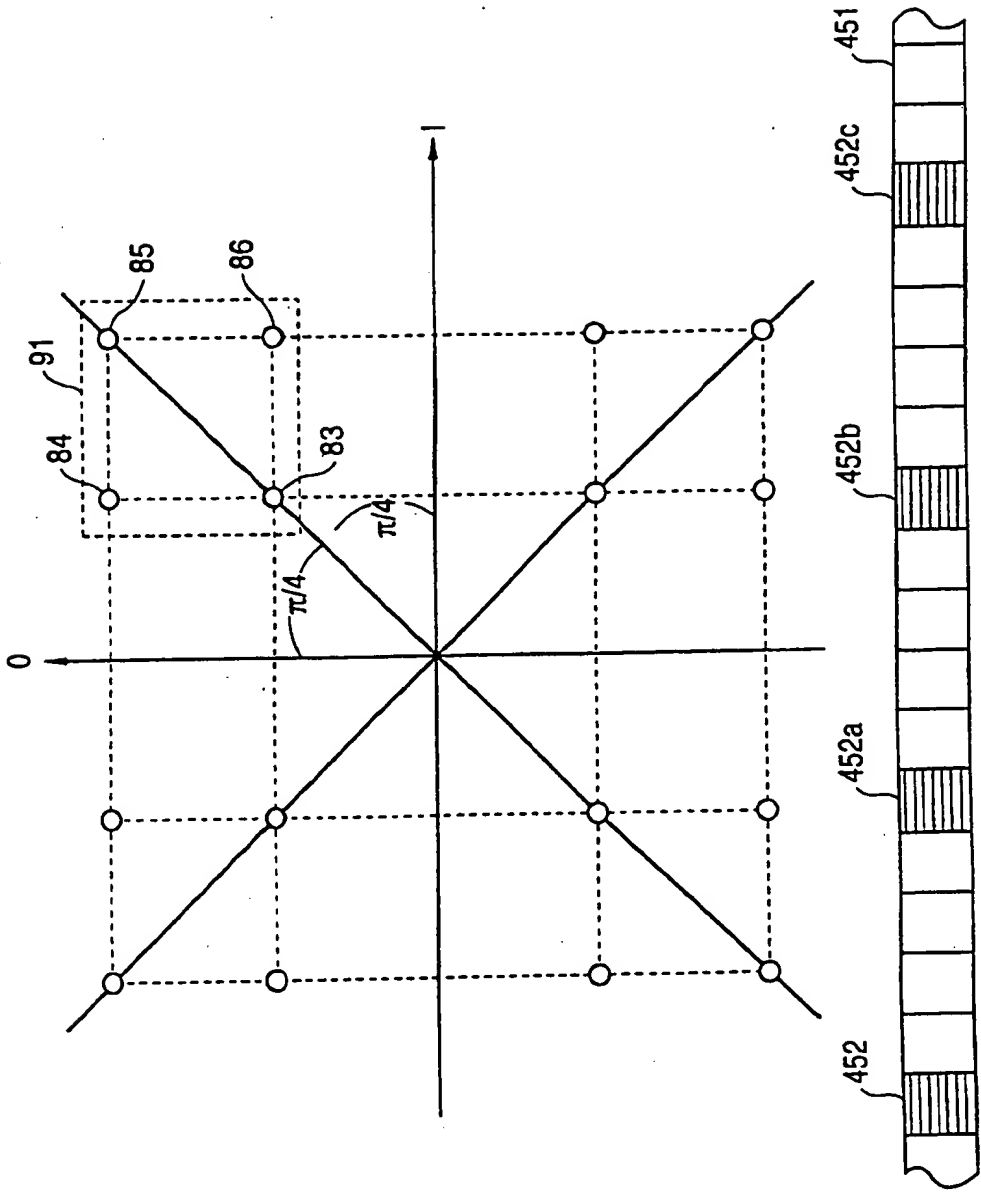
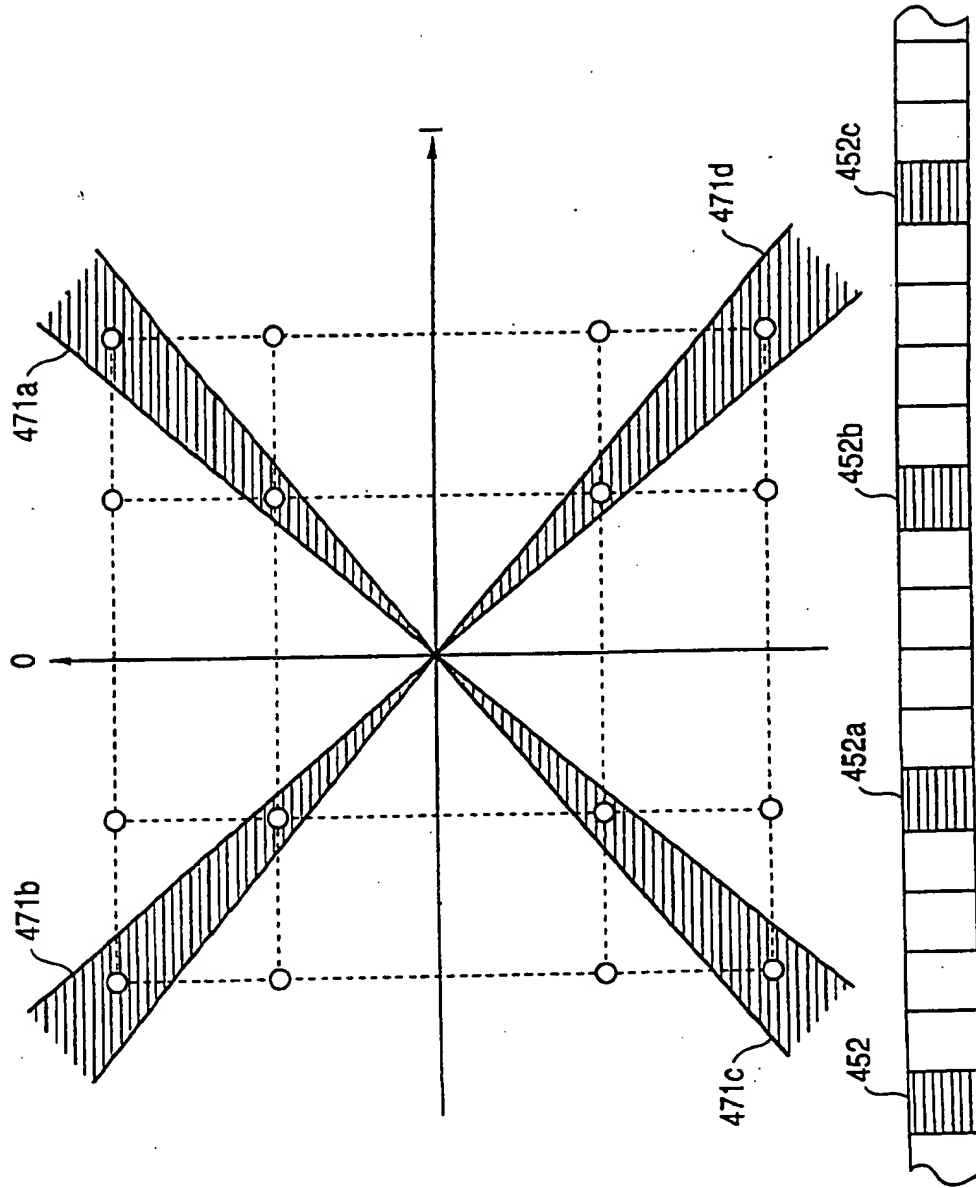
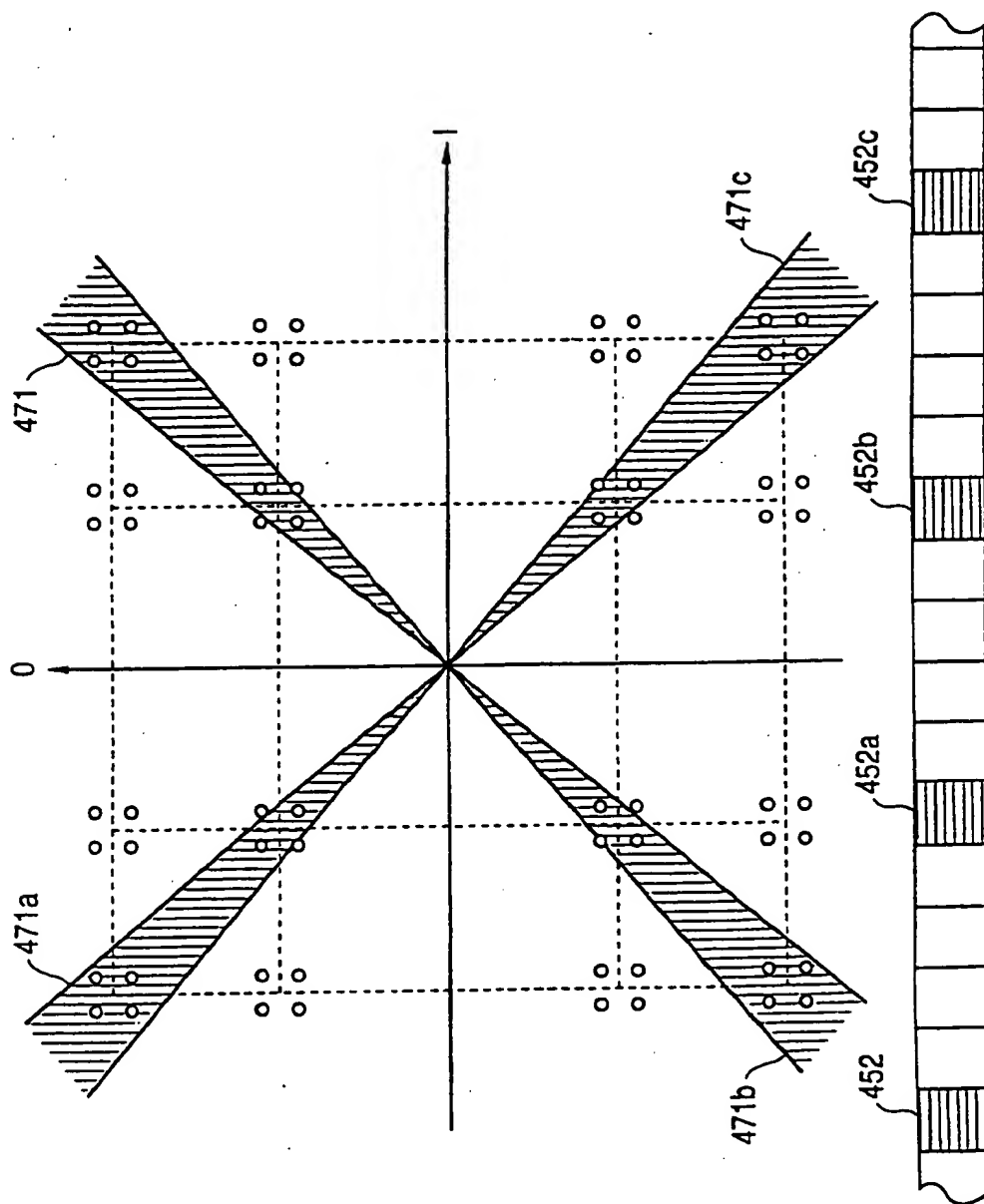


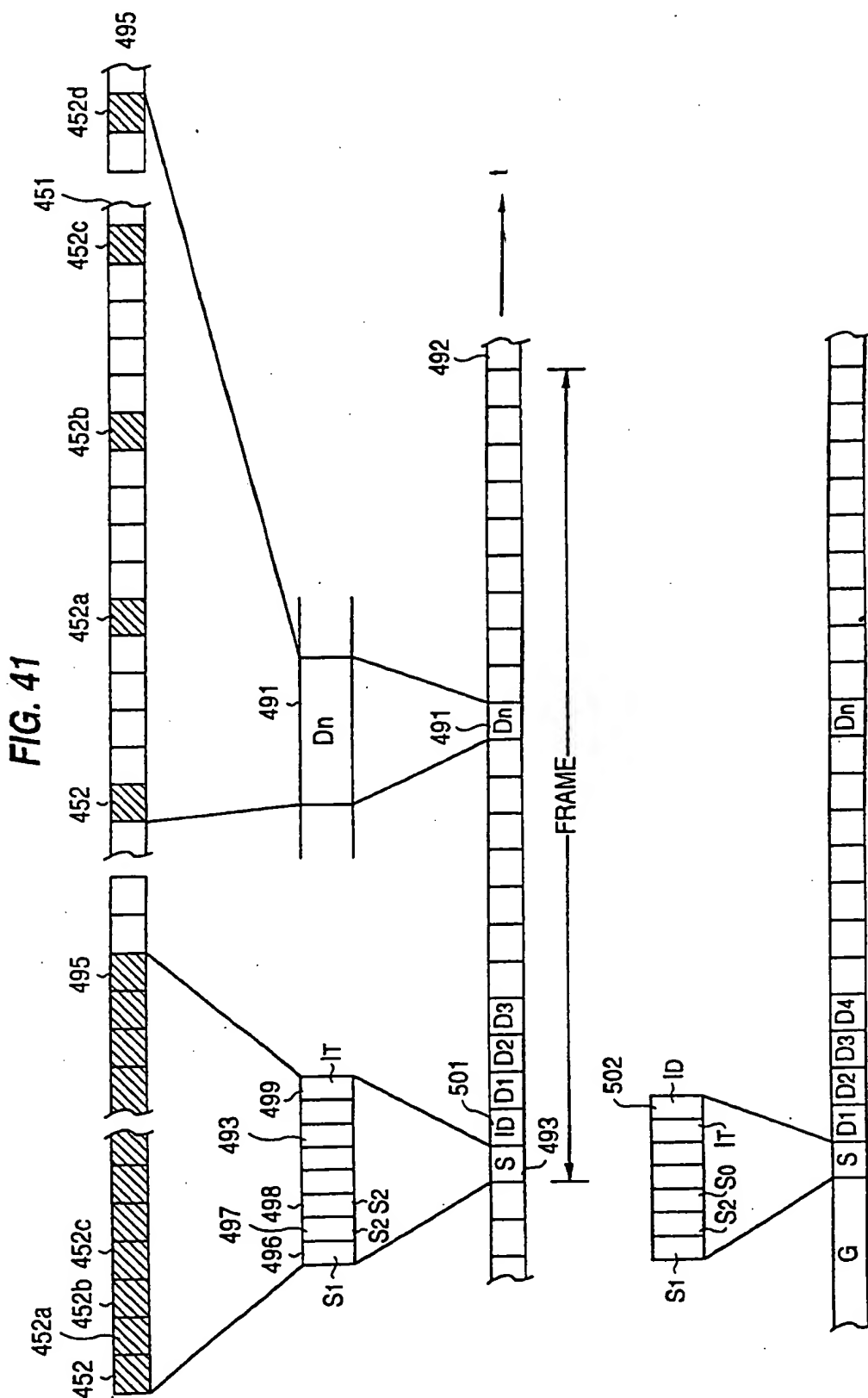
FIG. 39



005001-2708960

FIG. 40





**FIG. 42**

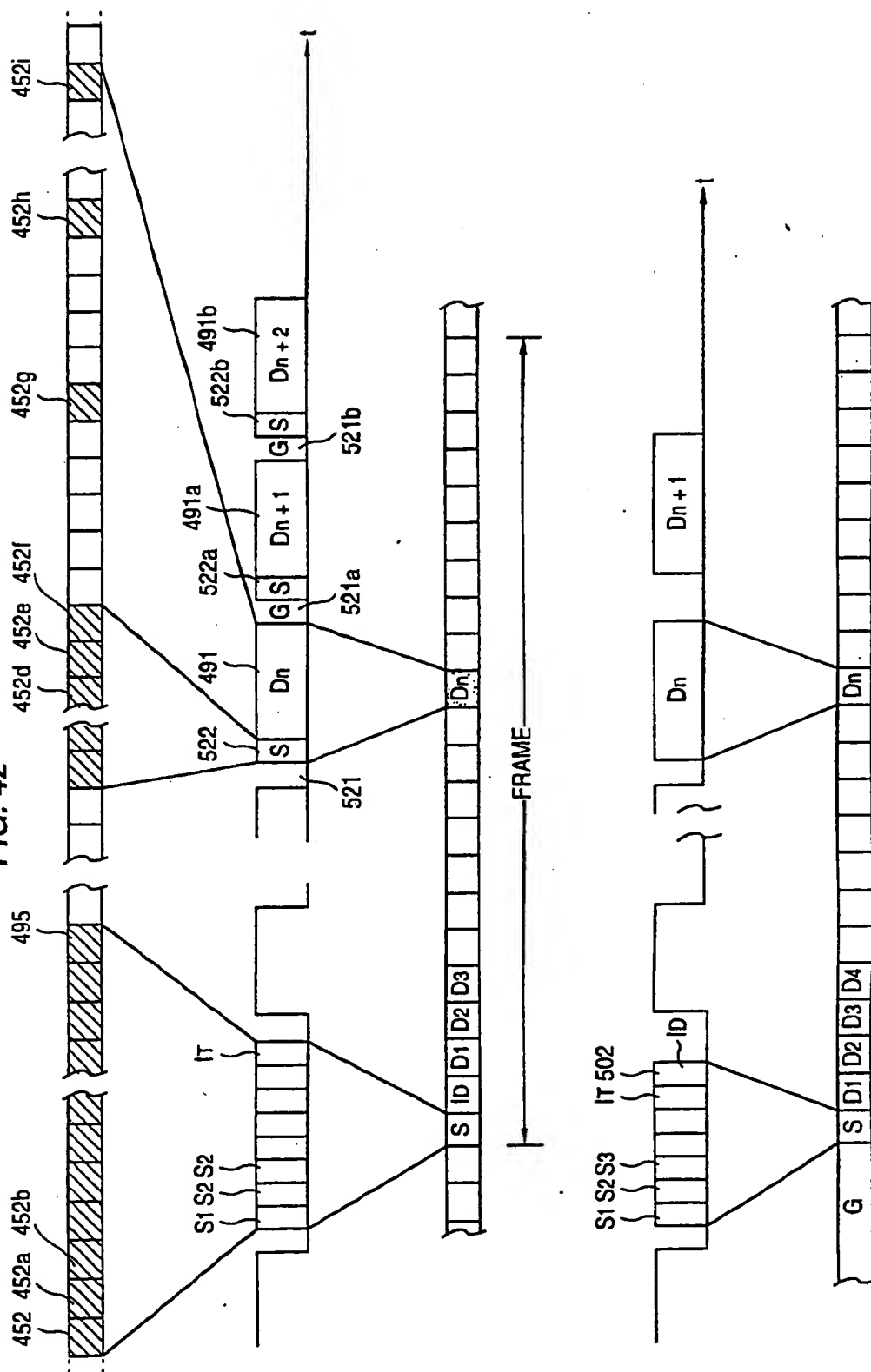
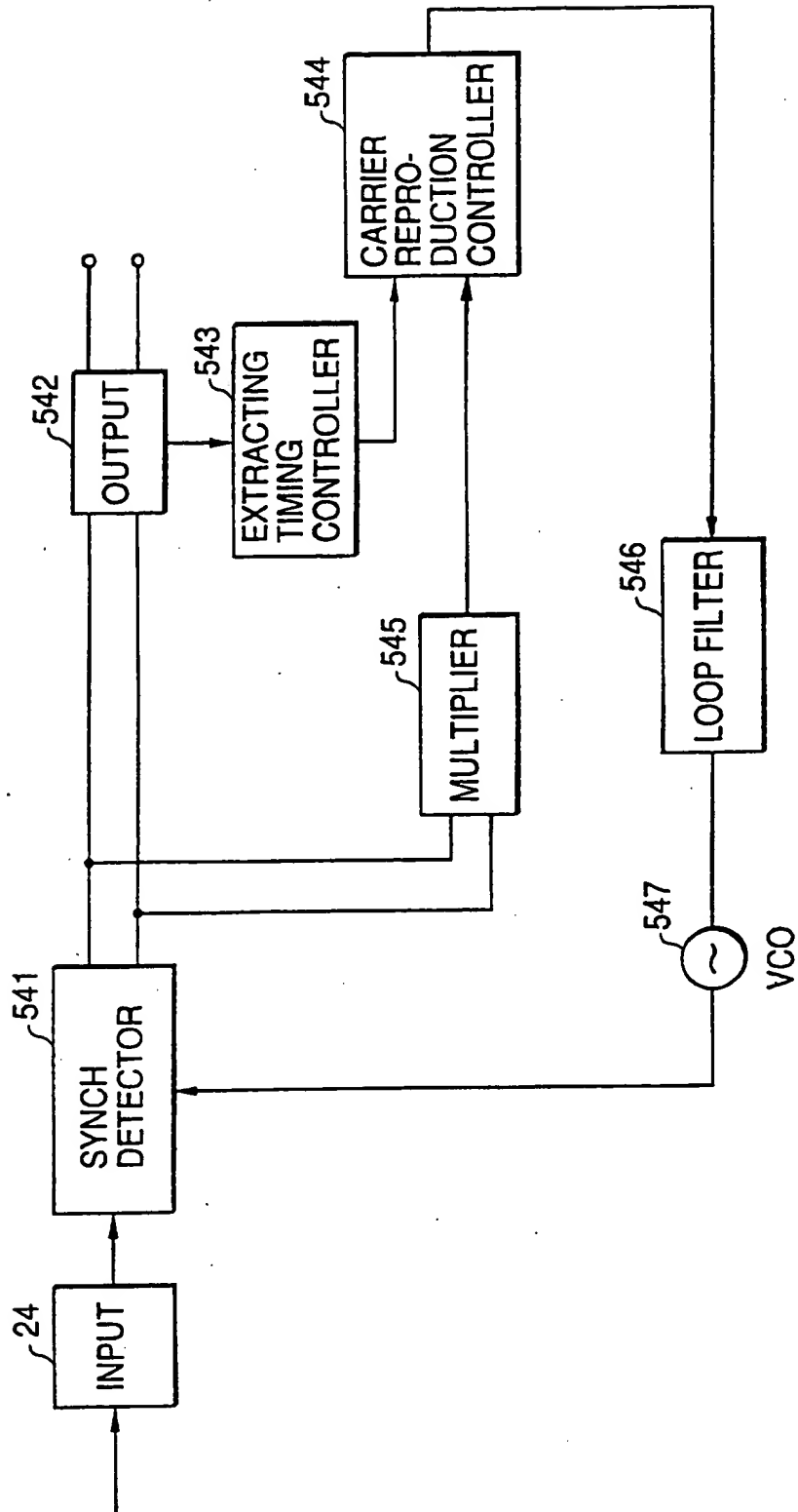


FIG. 43



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FIG. 44

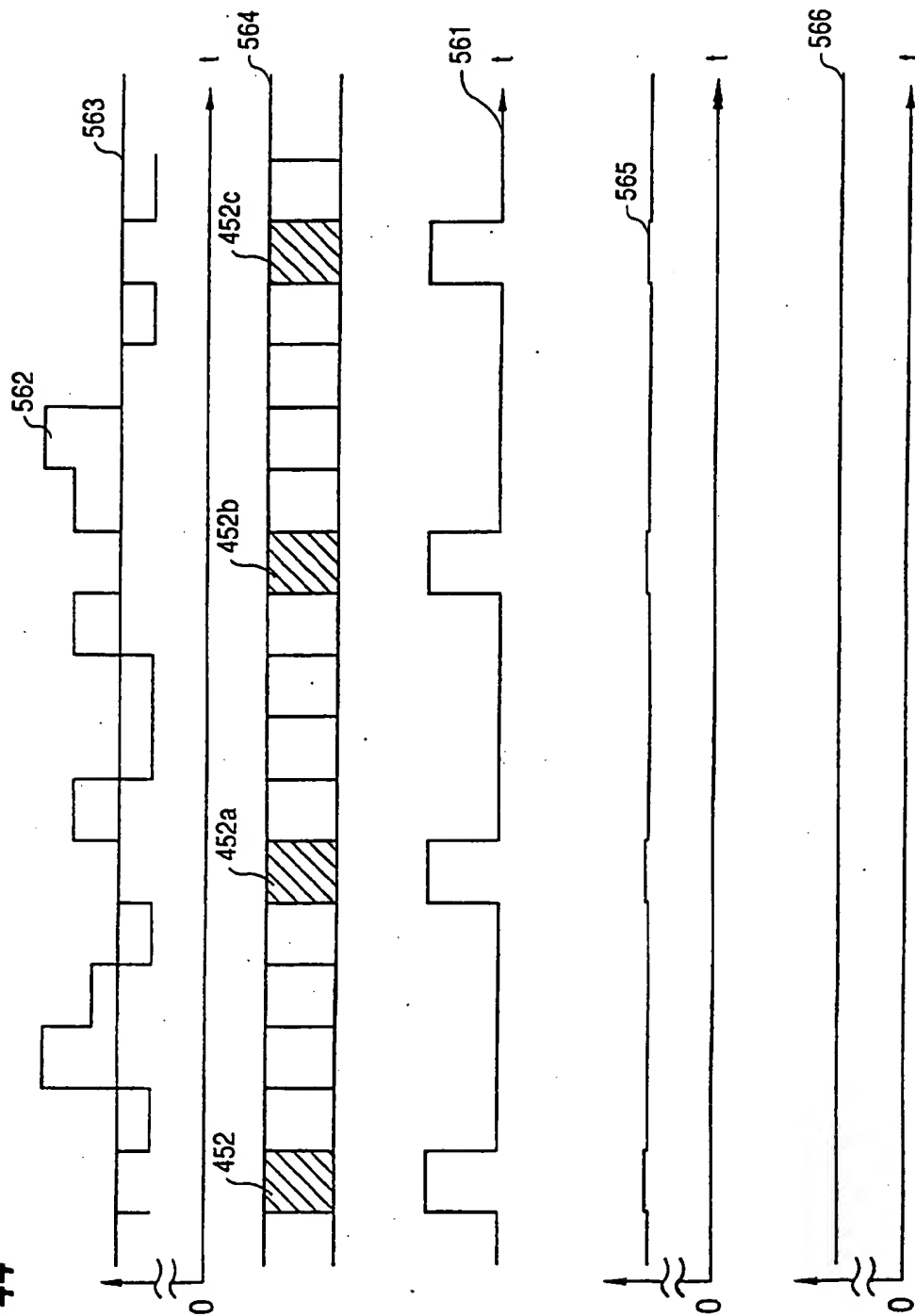


FIG. 45

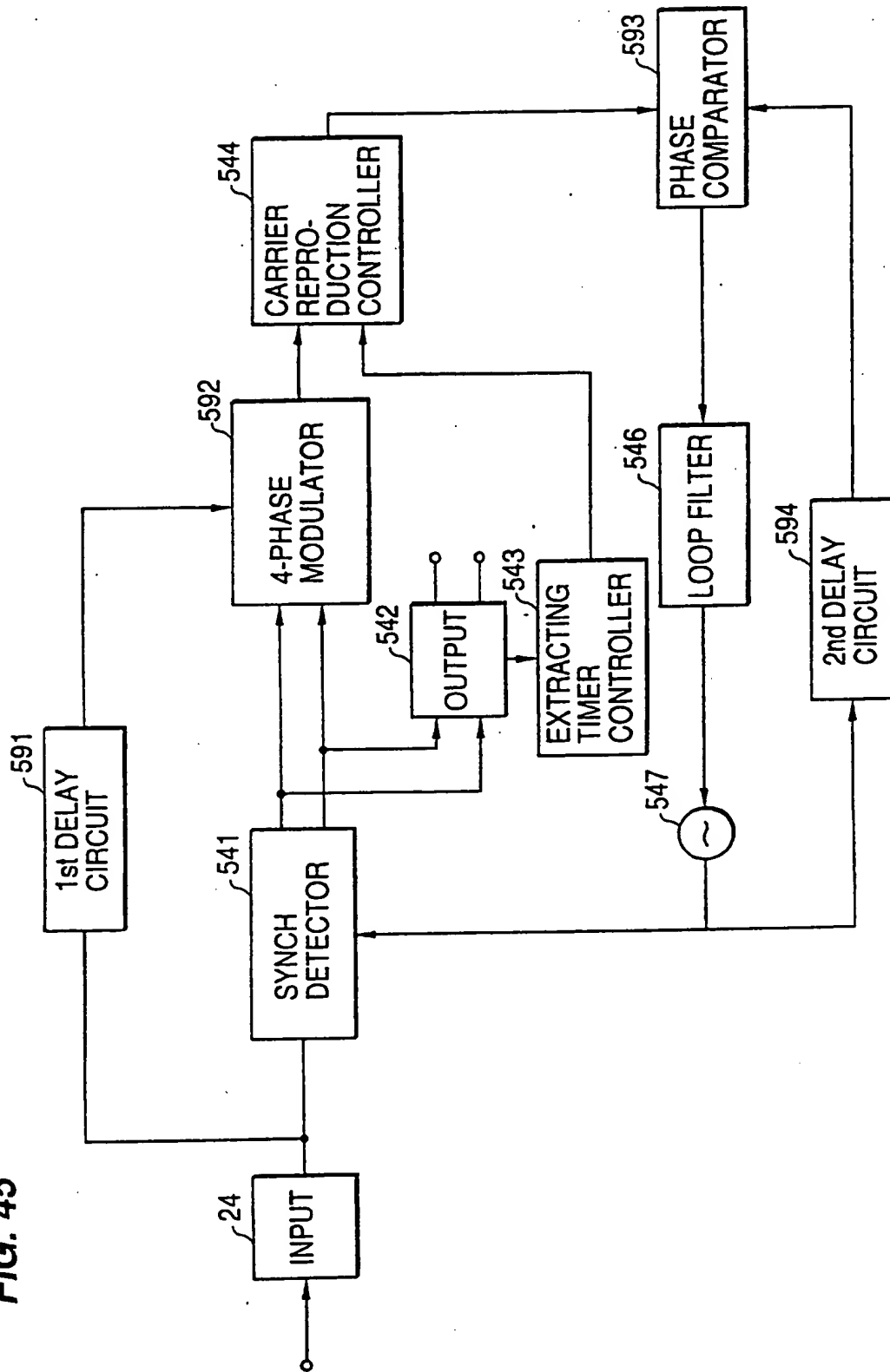


FIG. 46

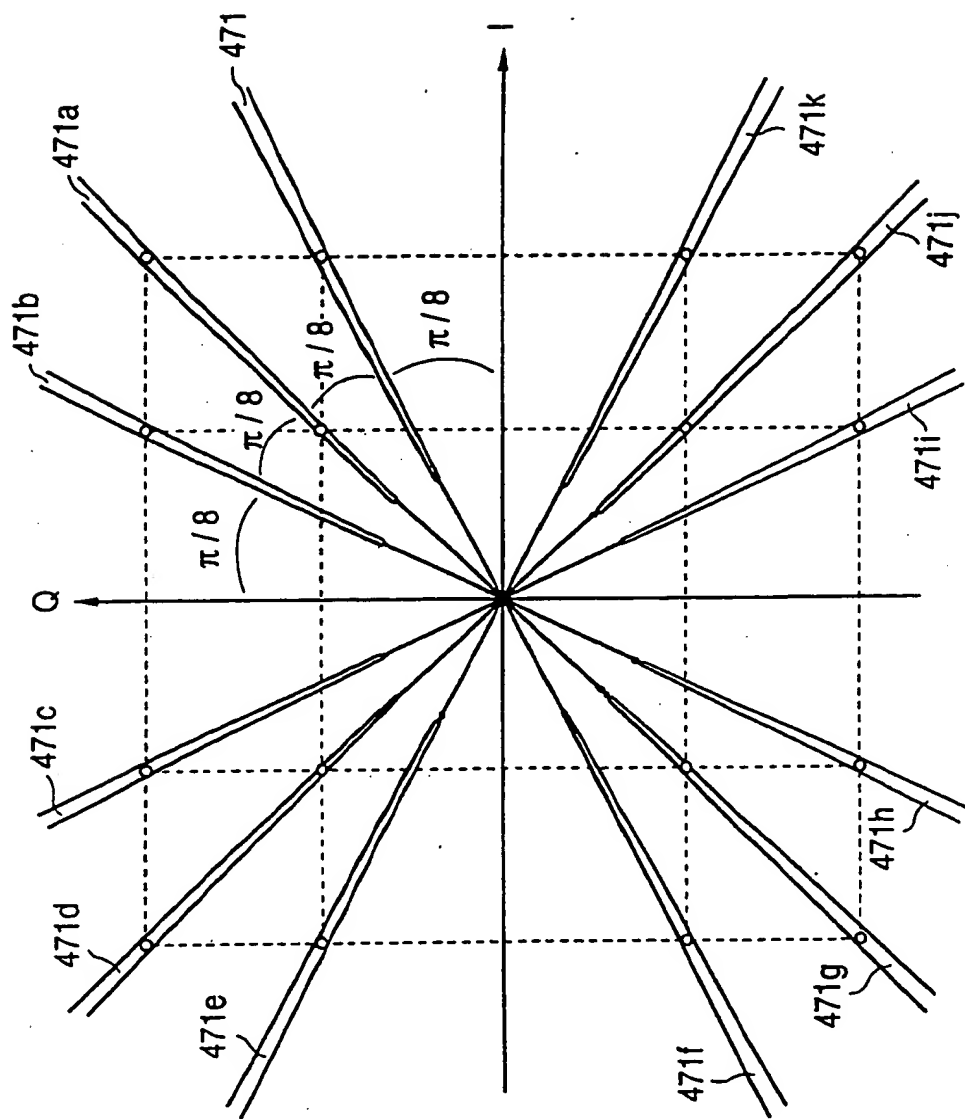


FIG. 47

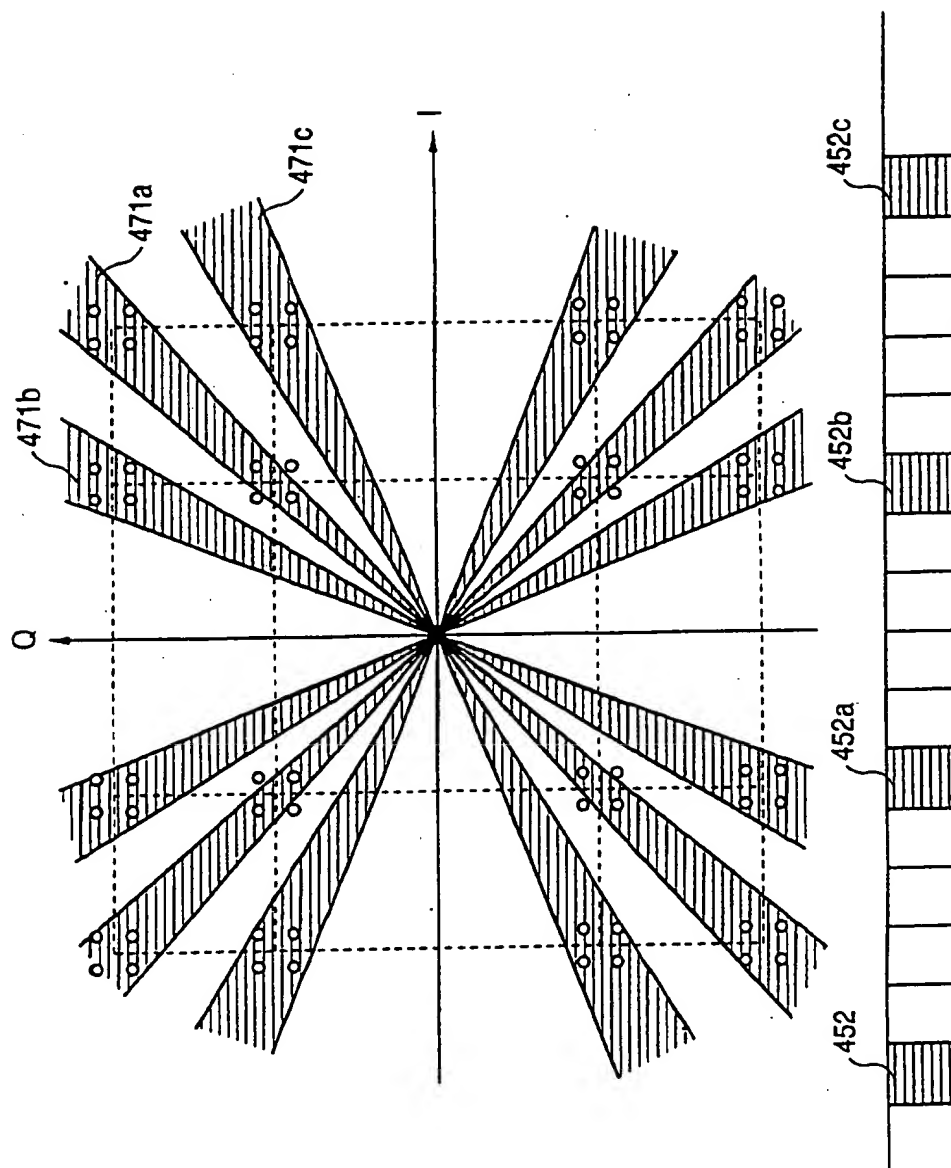


FIG. 48

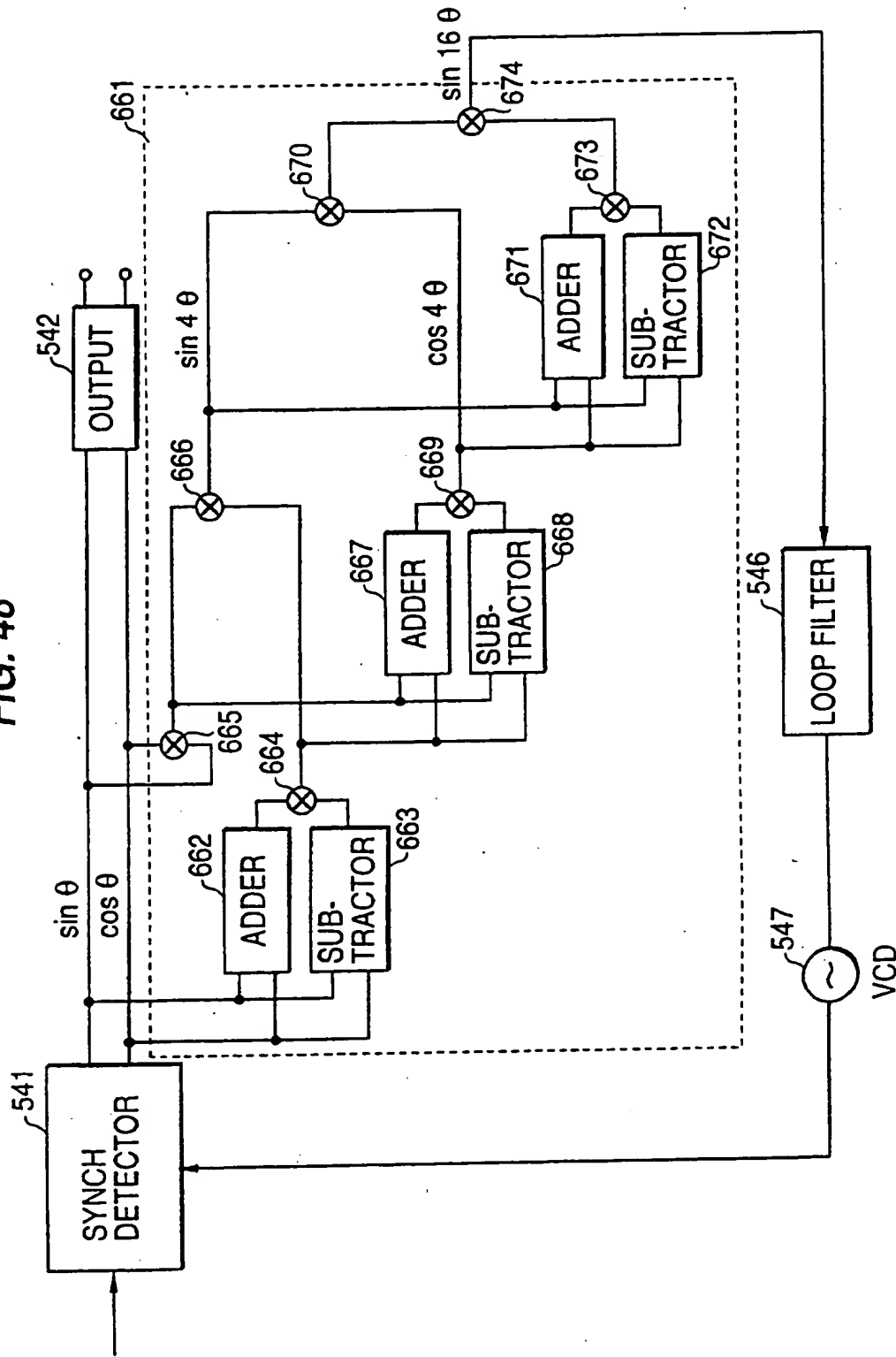


FIG. 49

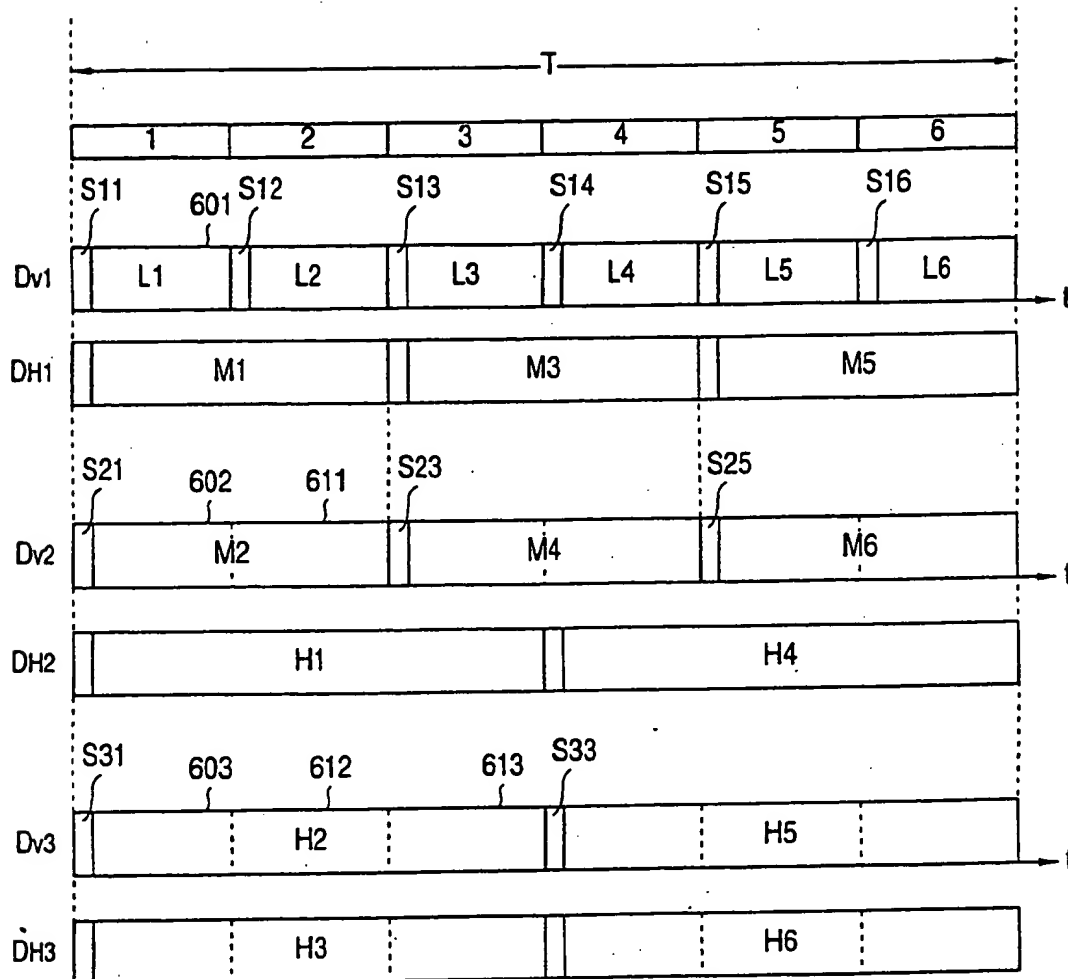
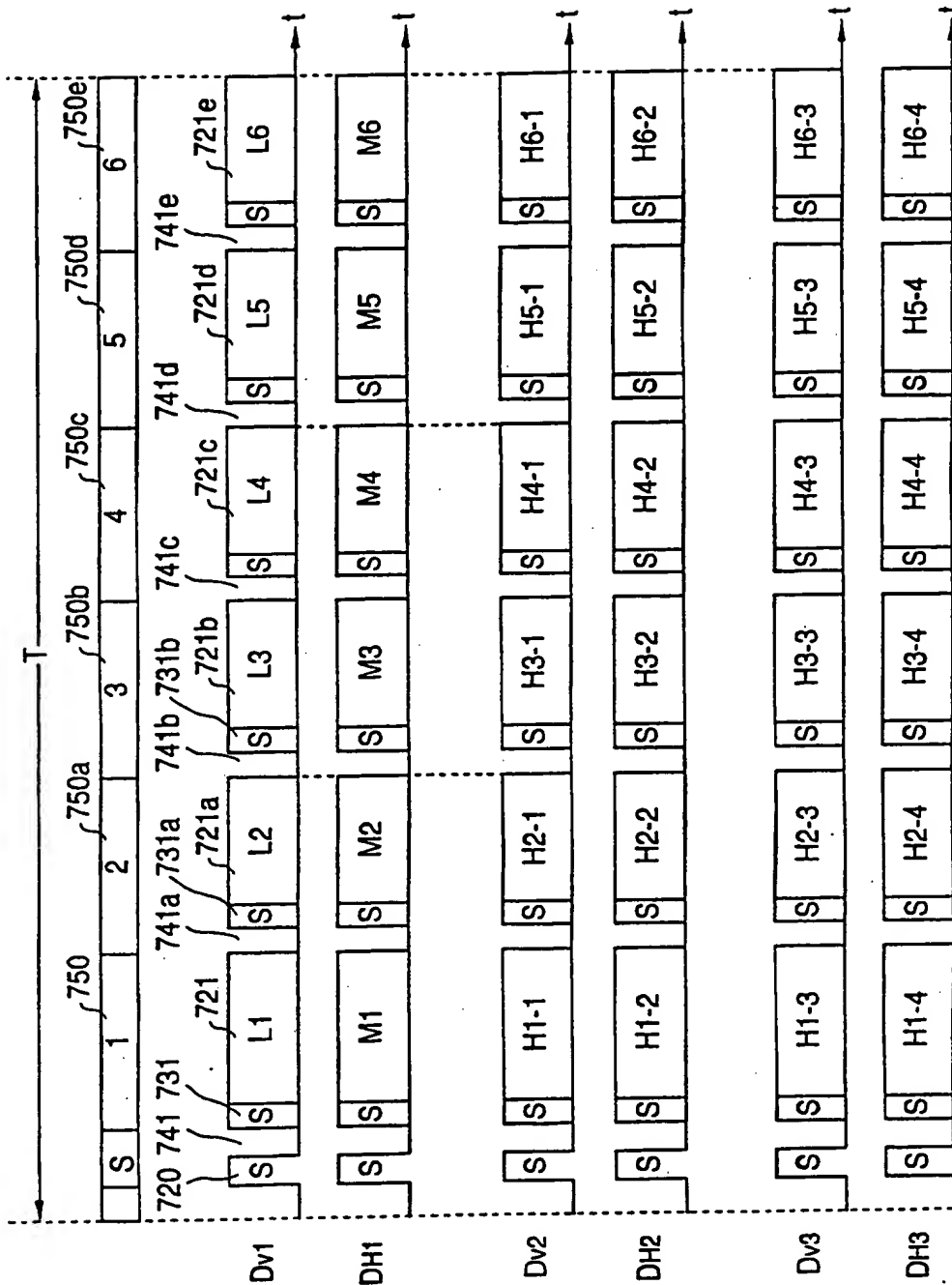


FIG. 50



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FIG. 51

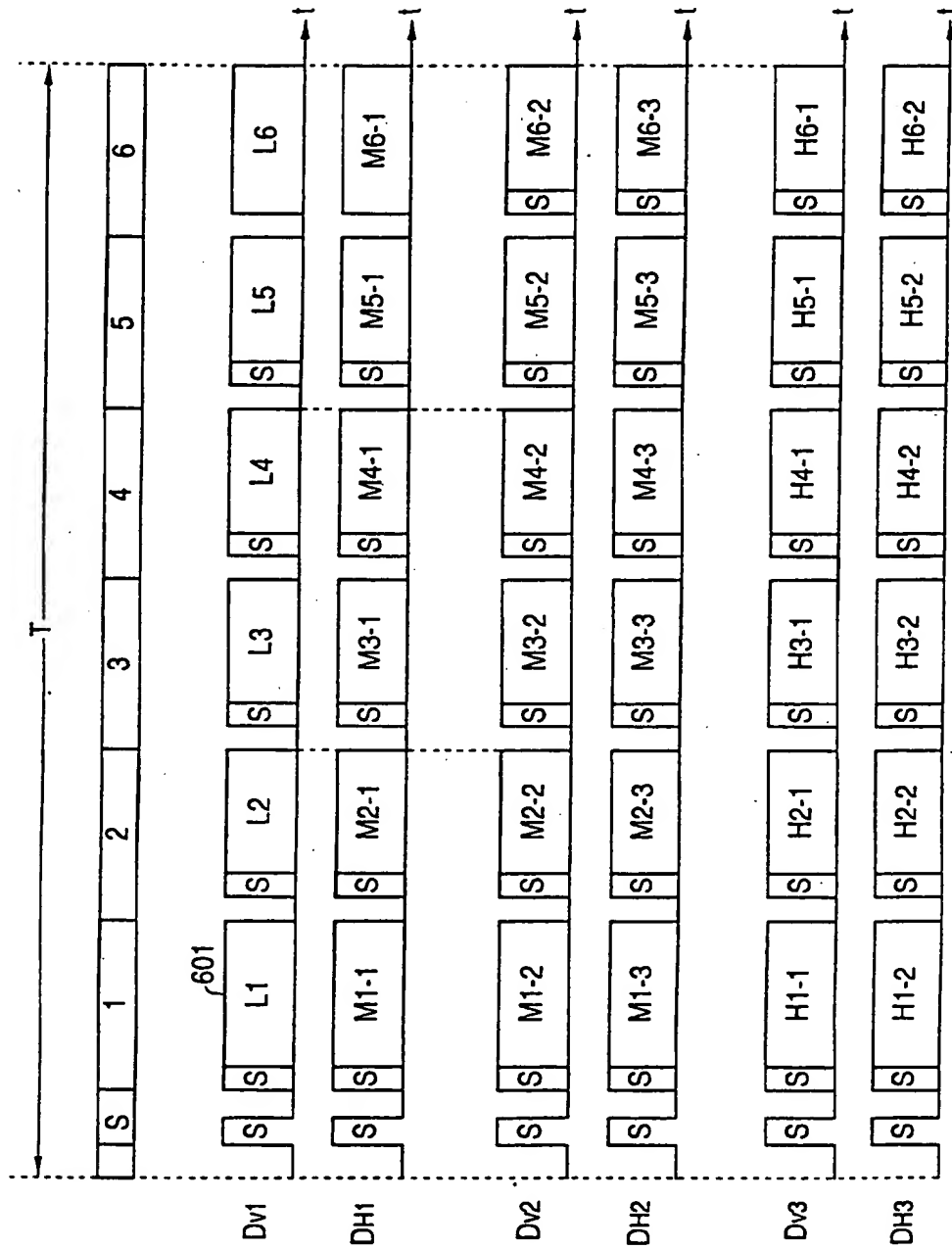
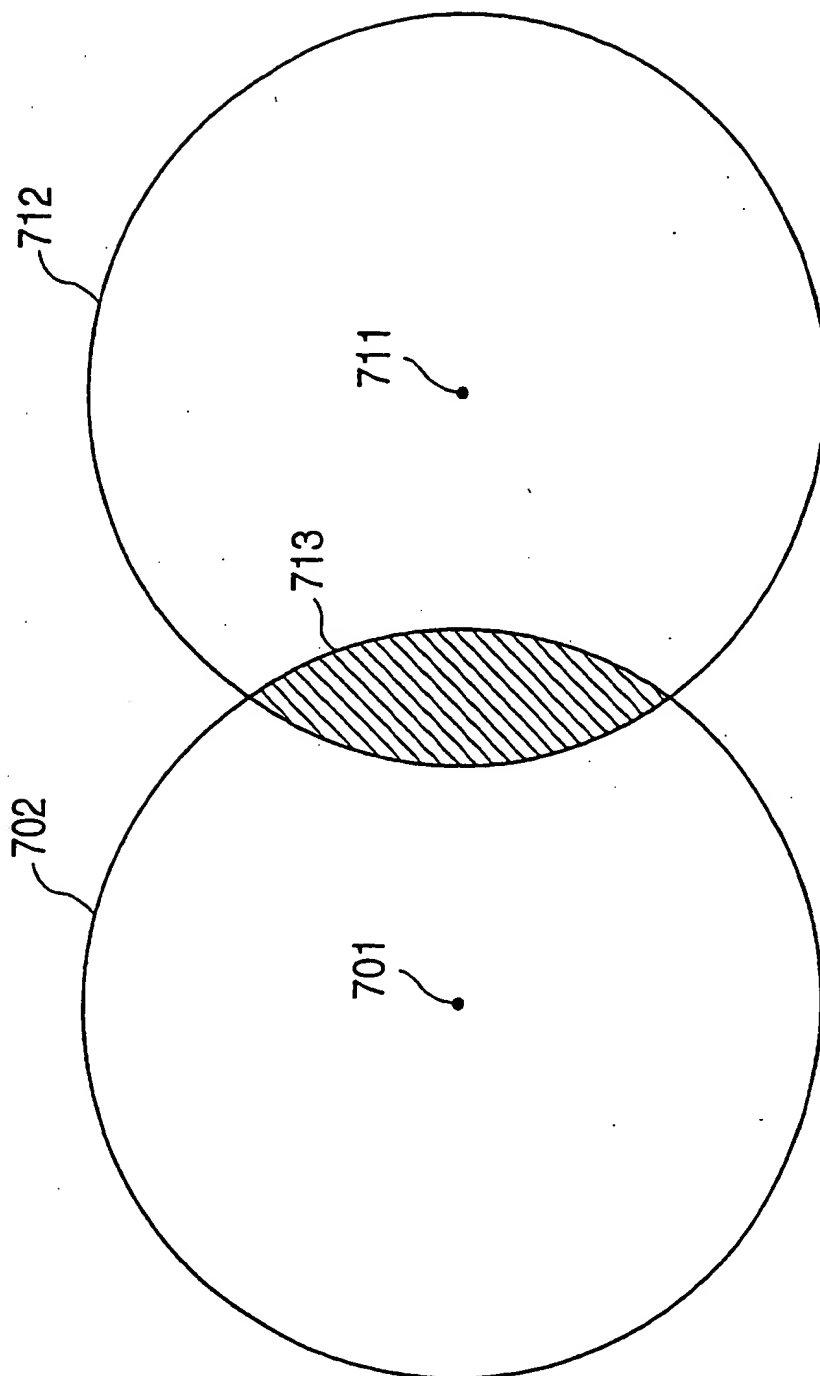
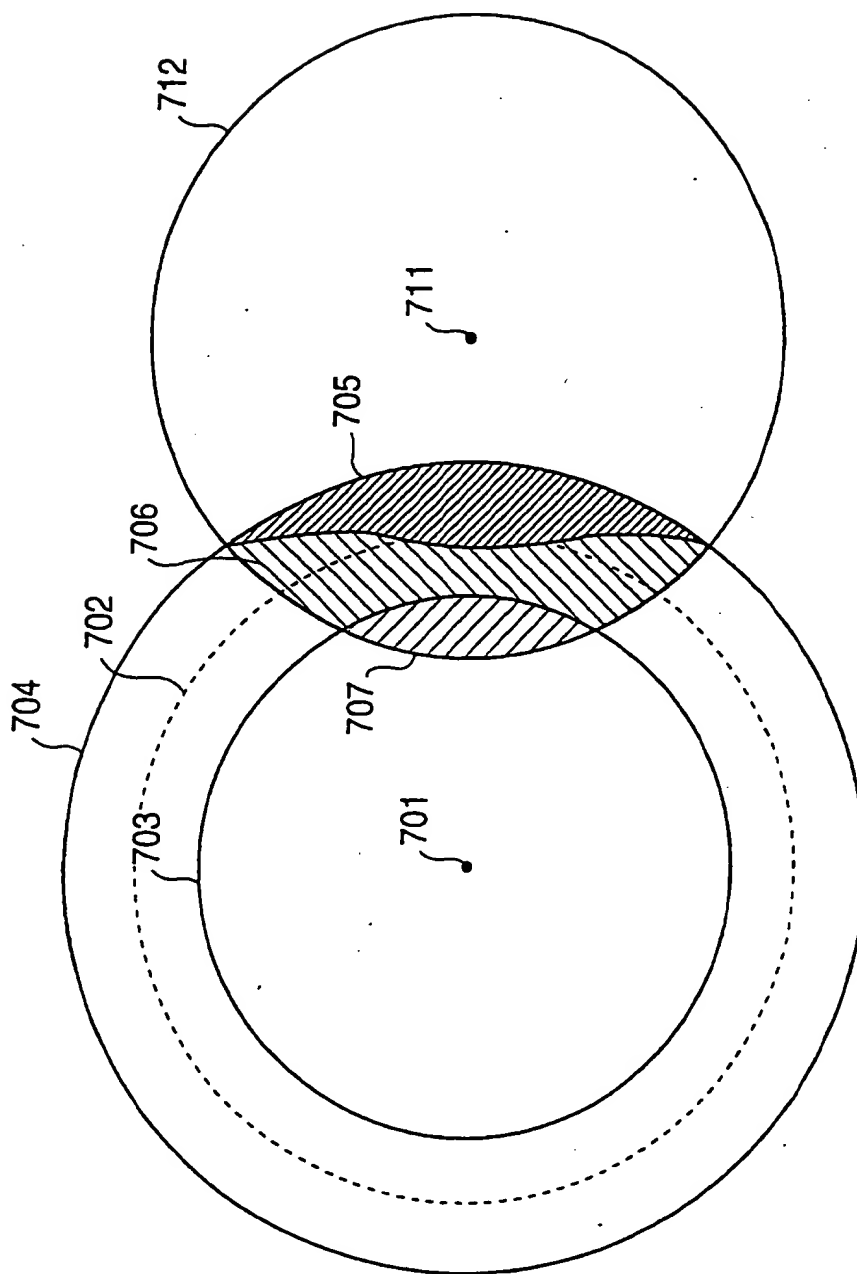


FIG. 52



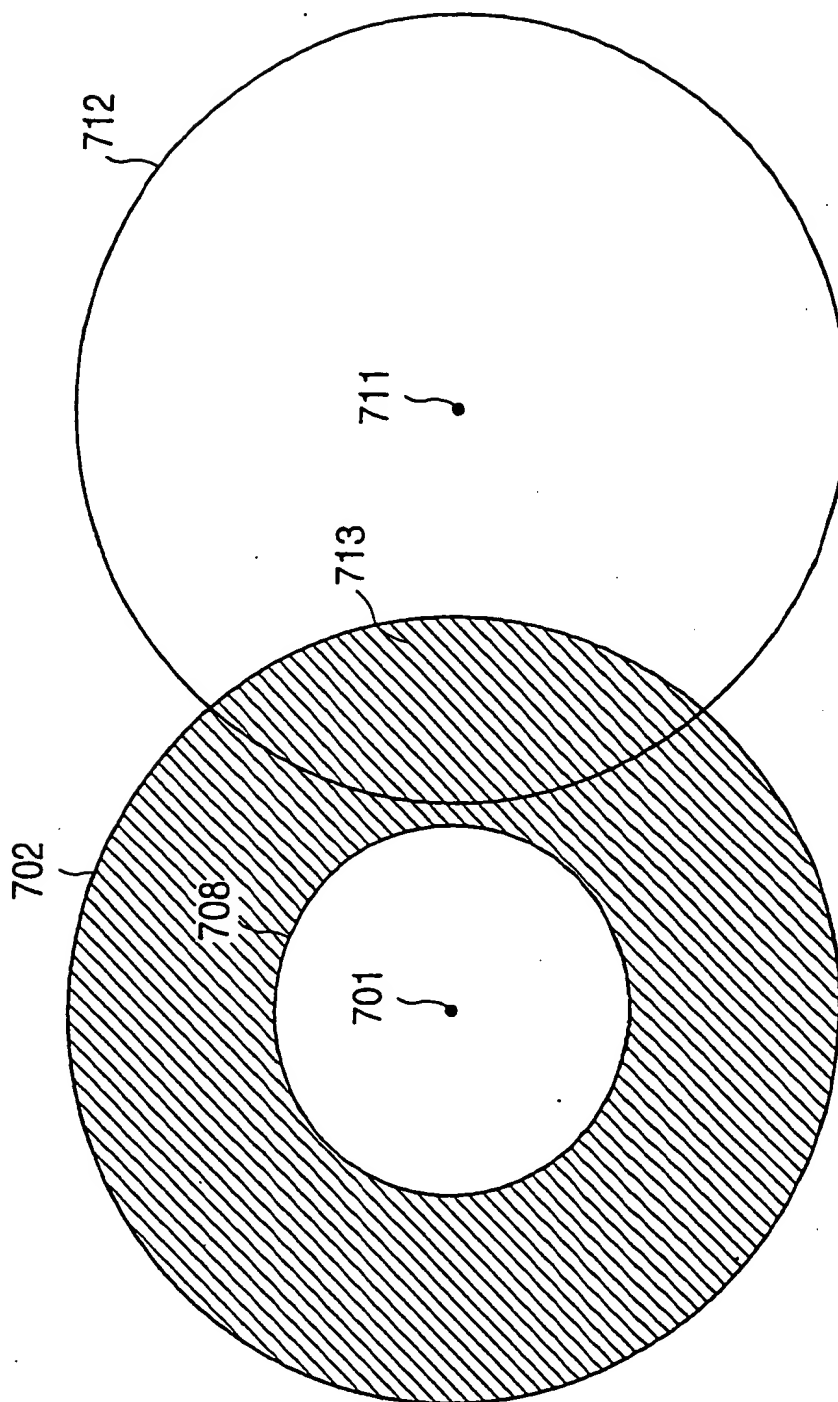
005007 2/203960

FIG. 53



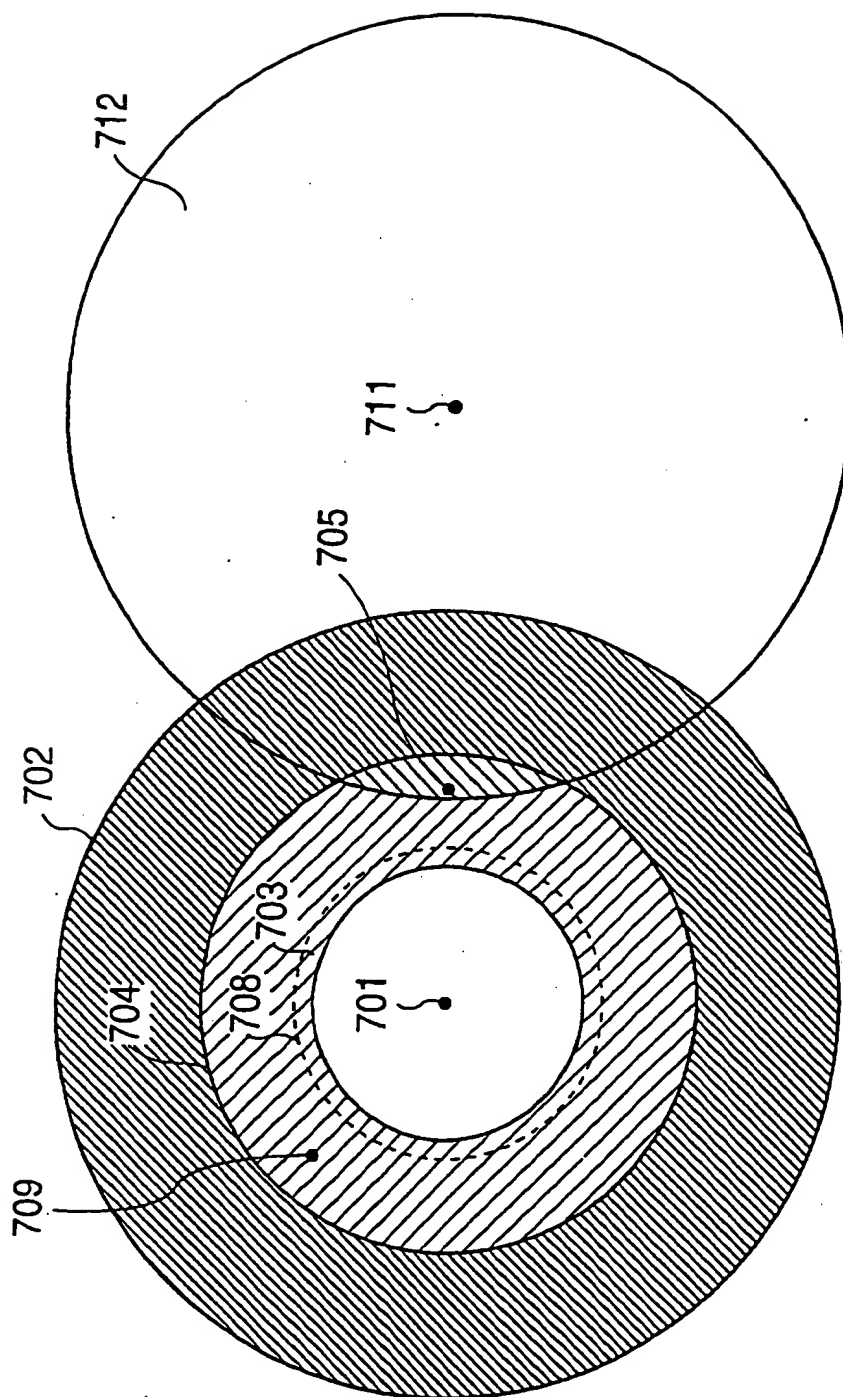
005097 2/1996

**FIG. 54**



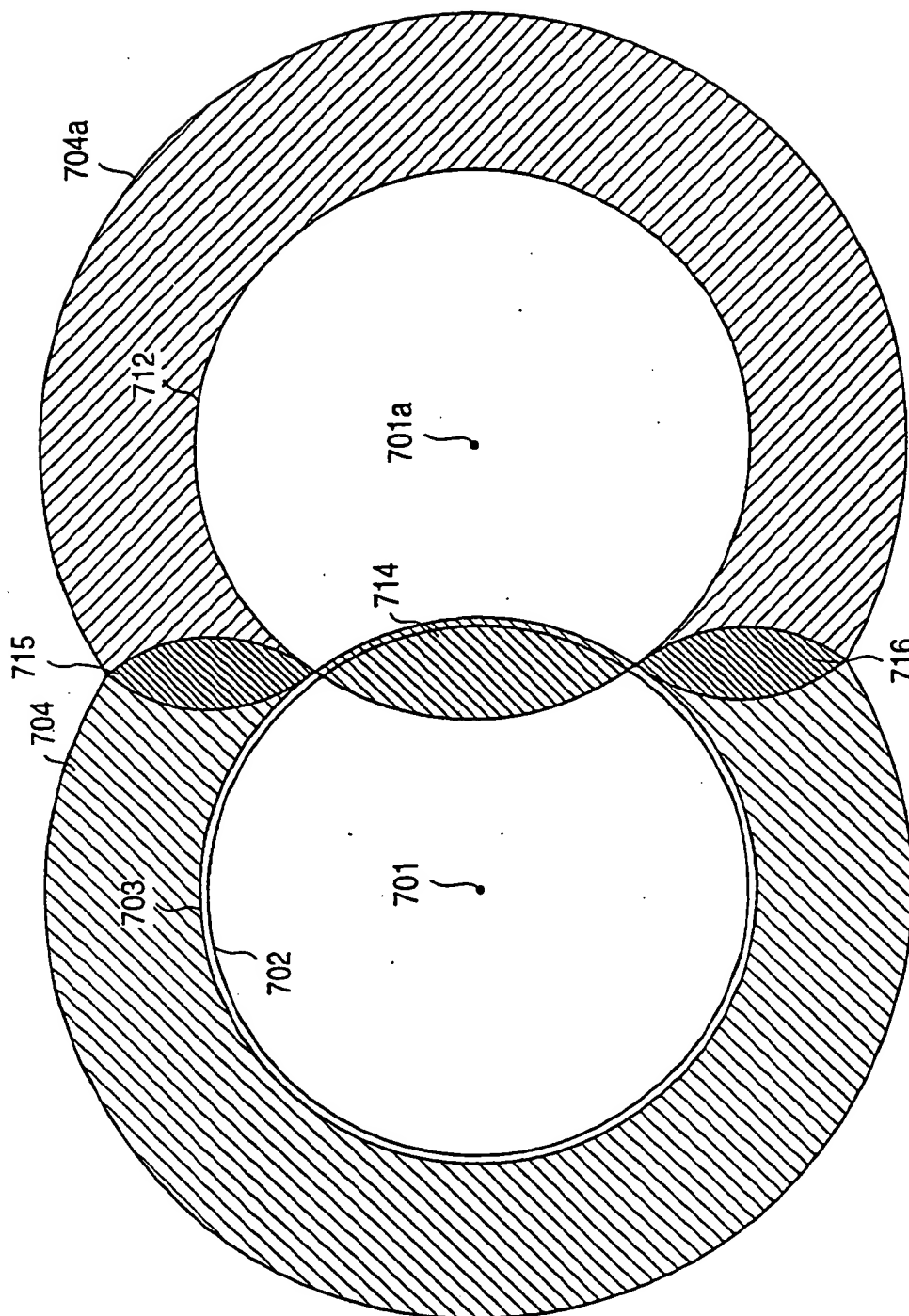
005001 / 100000

FIG. 55



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FIG. 56



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FIG. 57

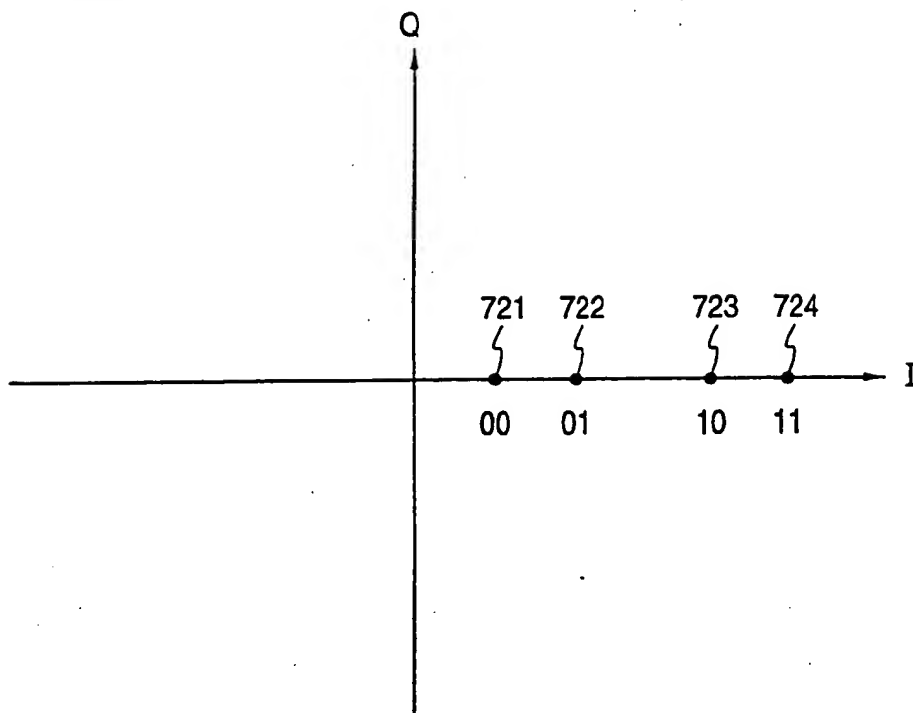


FIG. 58

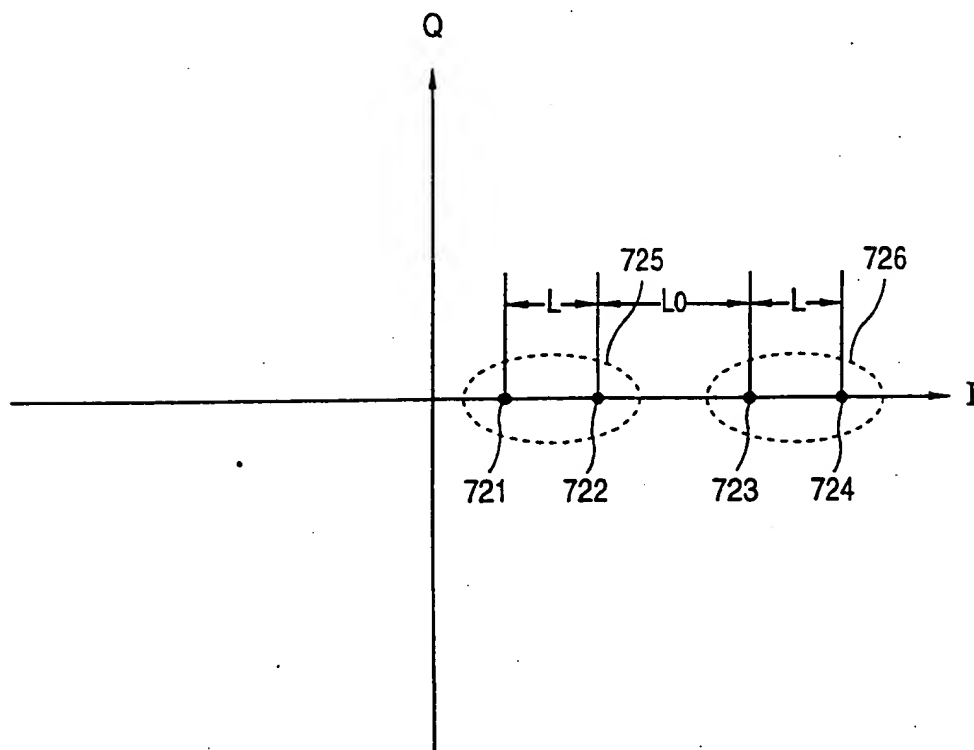


FIG. 59(a)

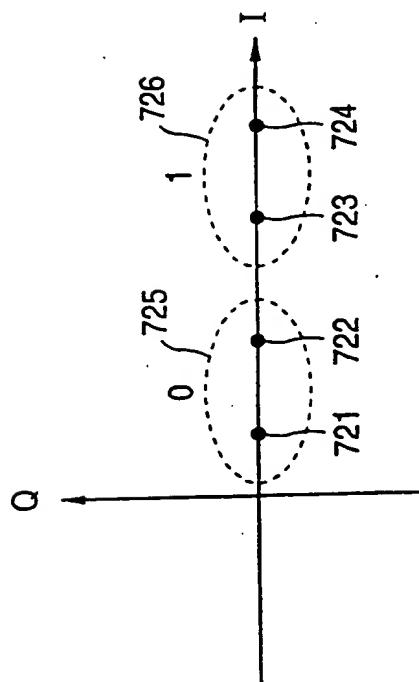


FIG. 59(b)

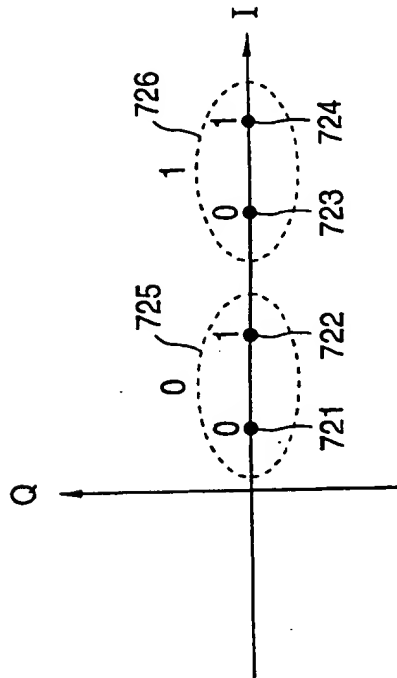


FIG. 59(c)

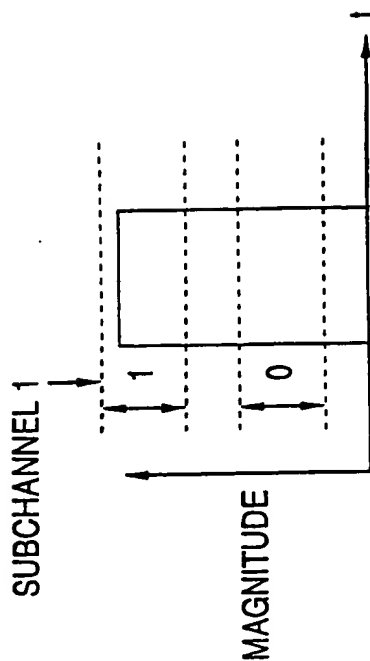


FIG. 59(d)

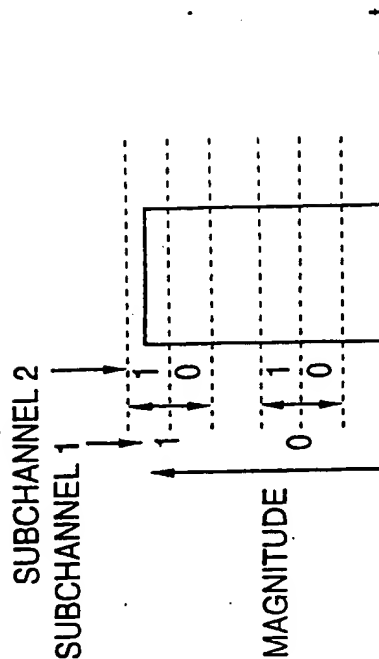


FIG. 59(a) / FIG. 59(b)

FIG. 60

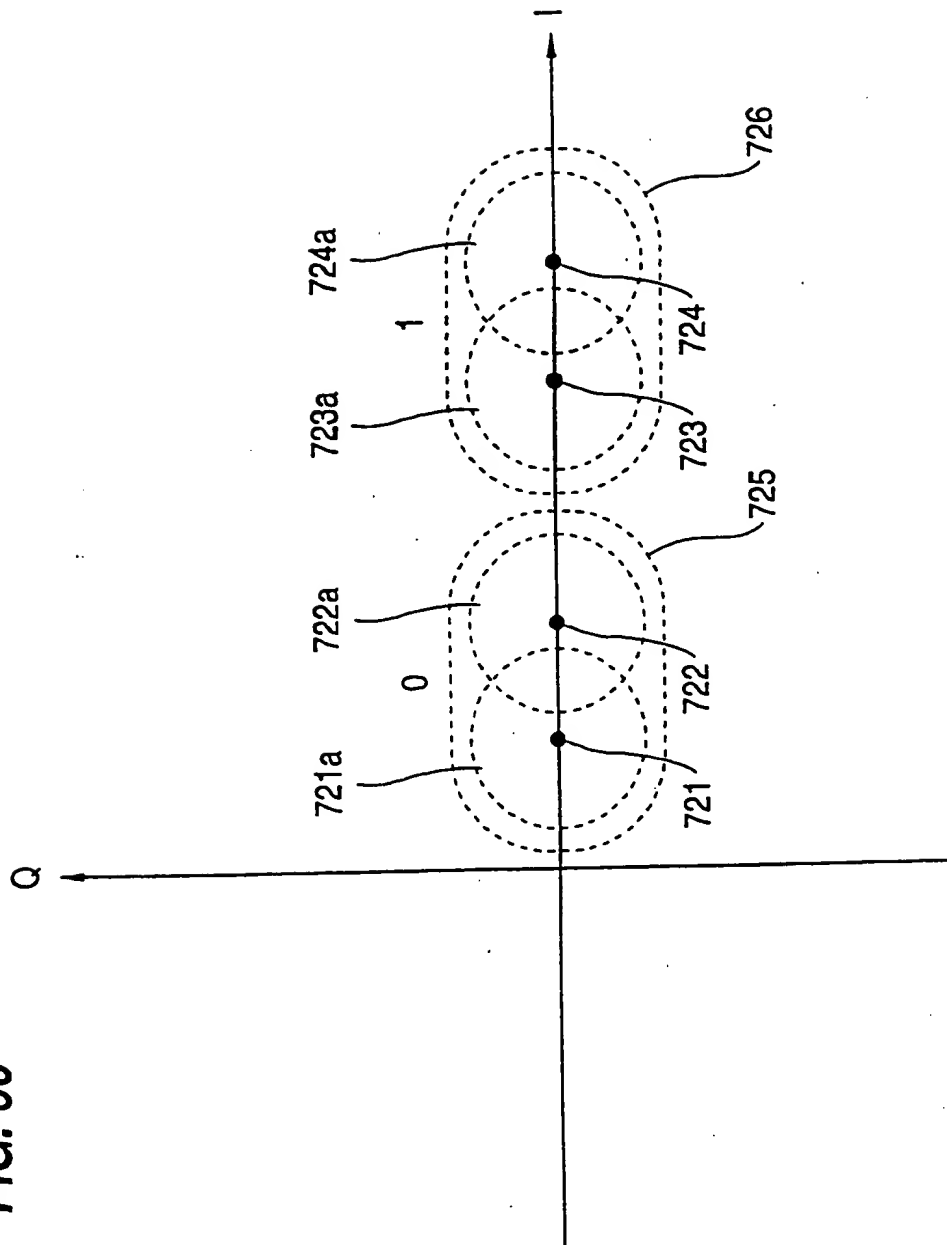


FIG. 61

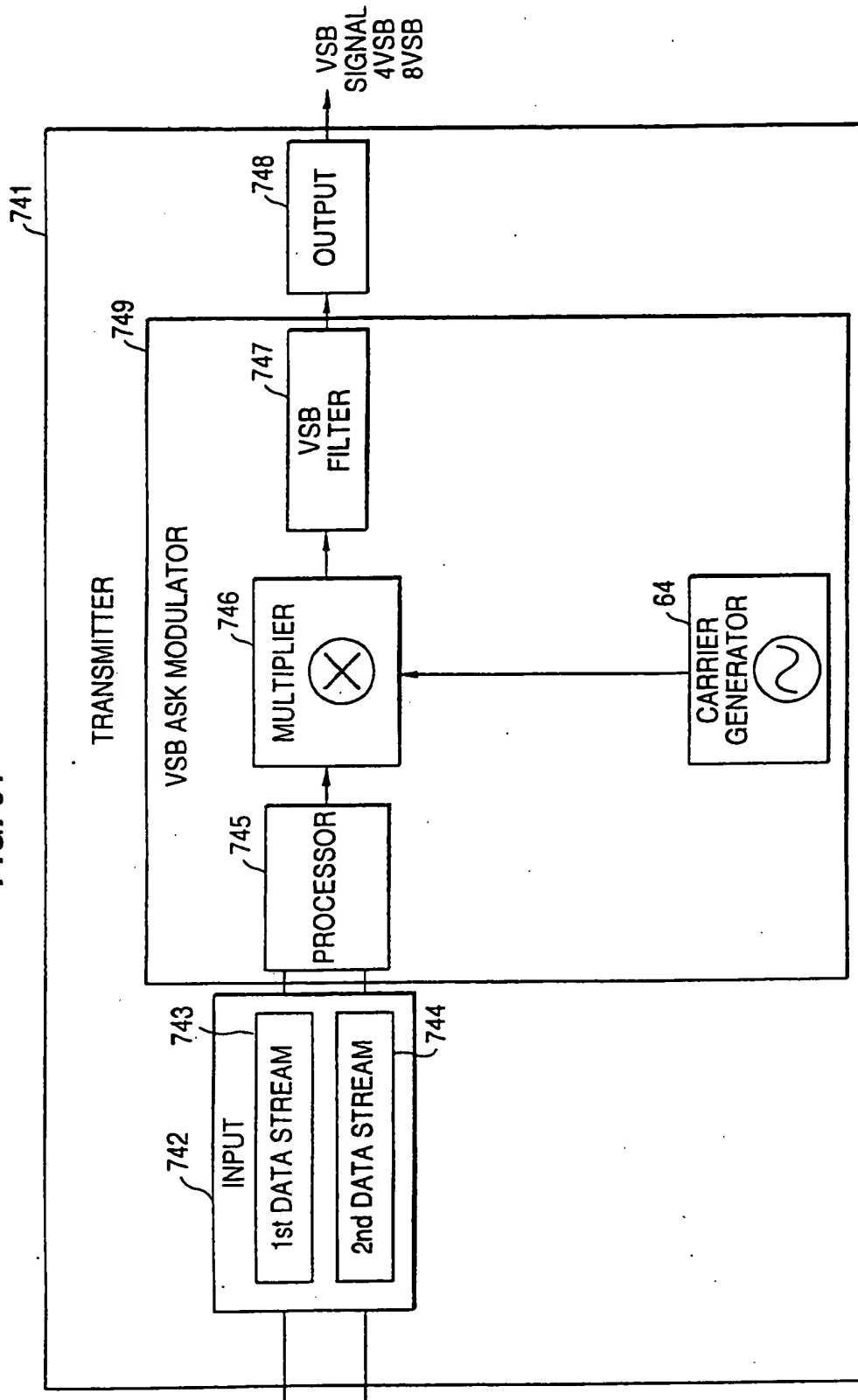


FIG. 62(a)

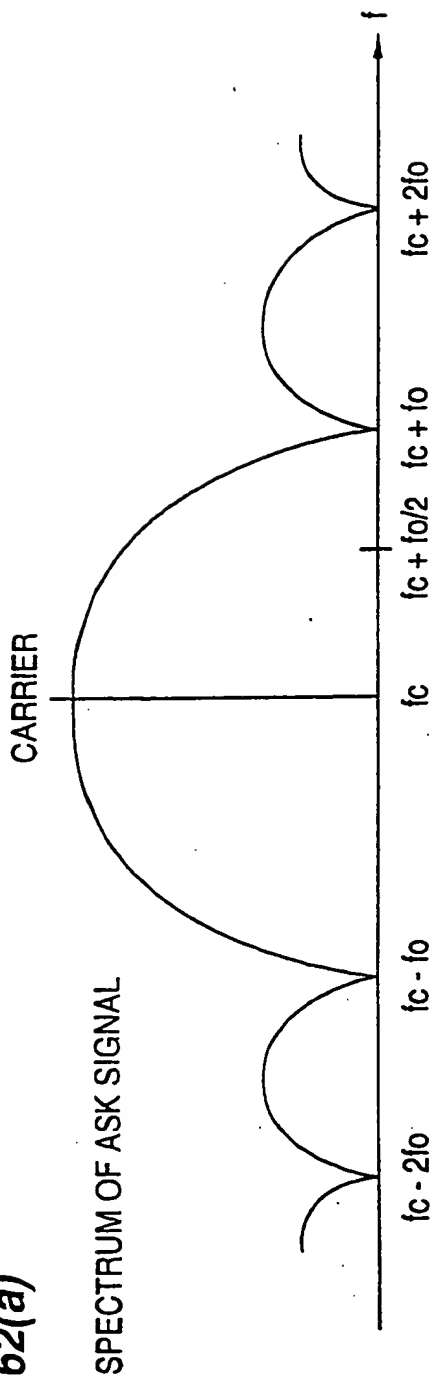


FIG. 62(b)

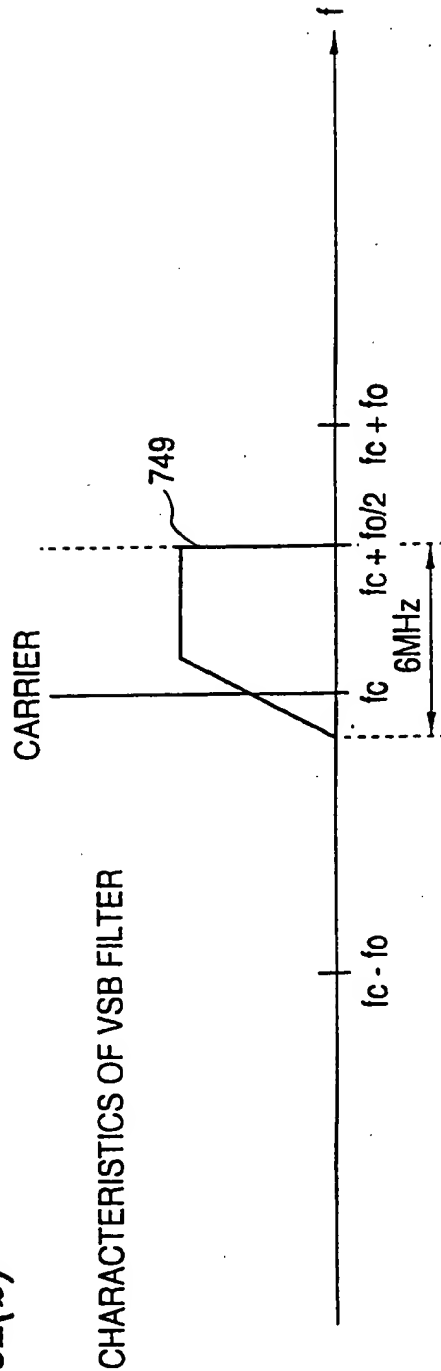


FIG. 63

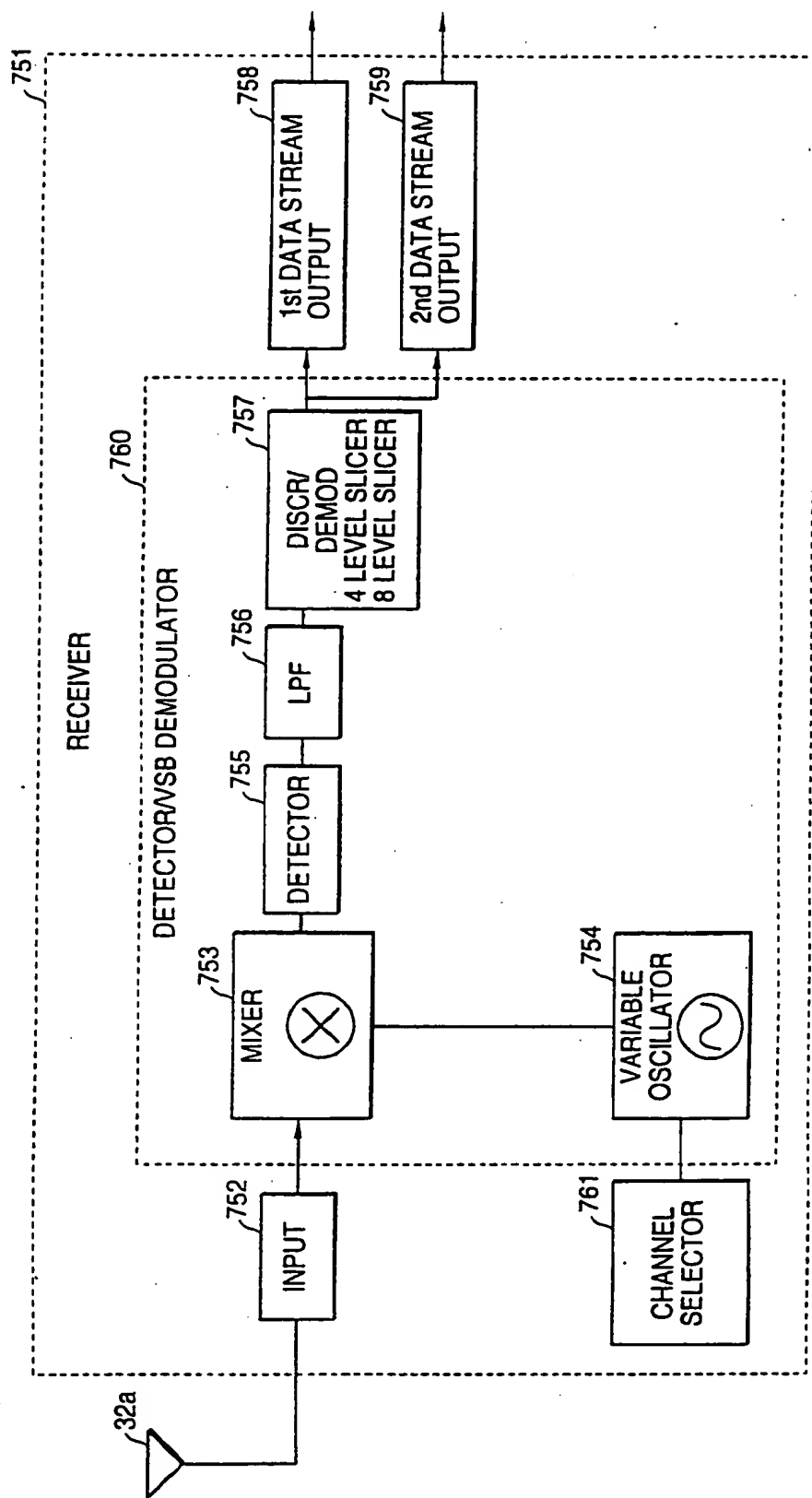


FIG. 64

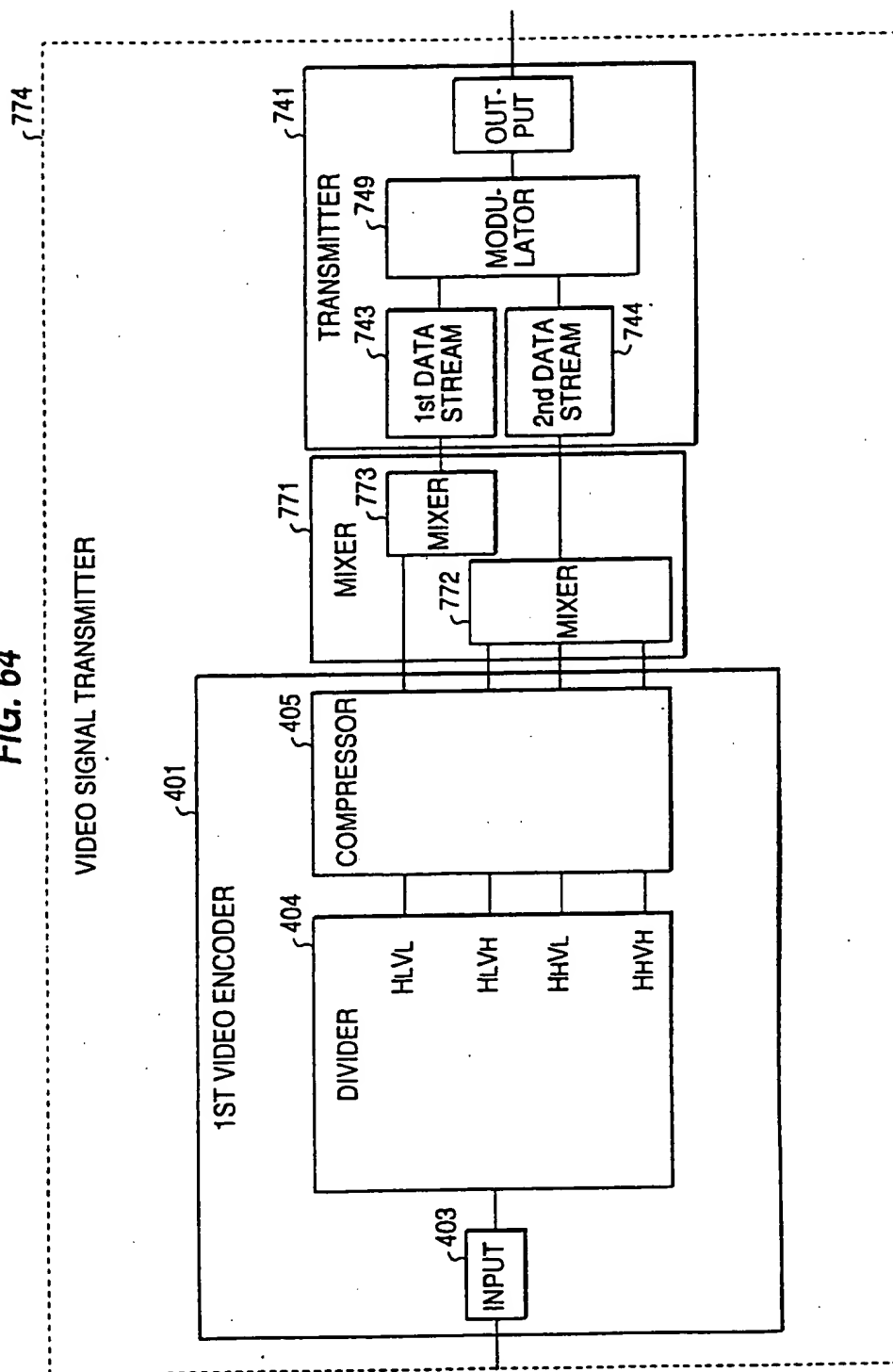


FIG. 65

FIG. 65

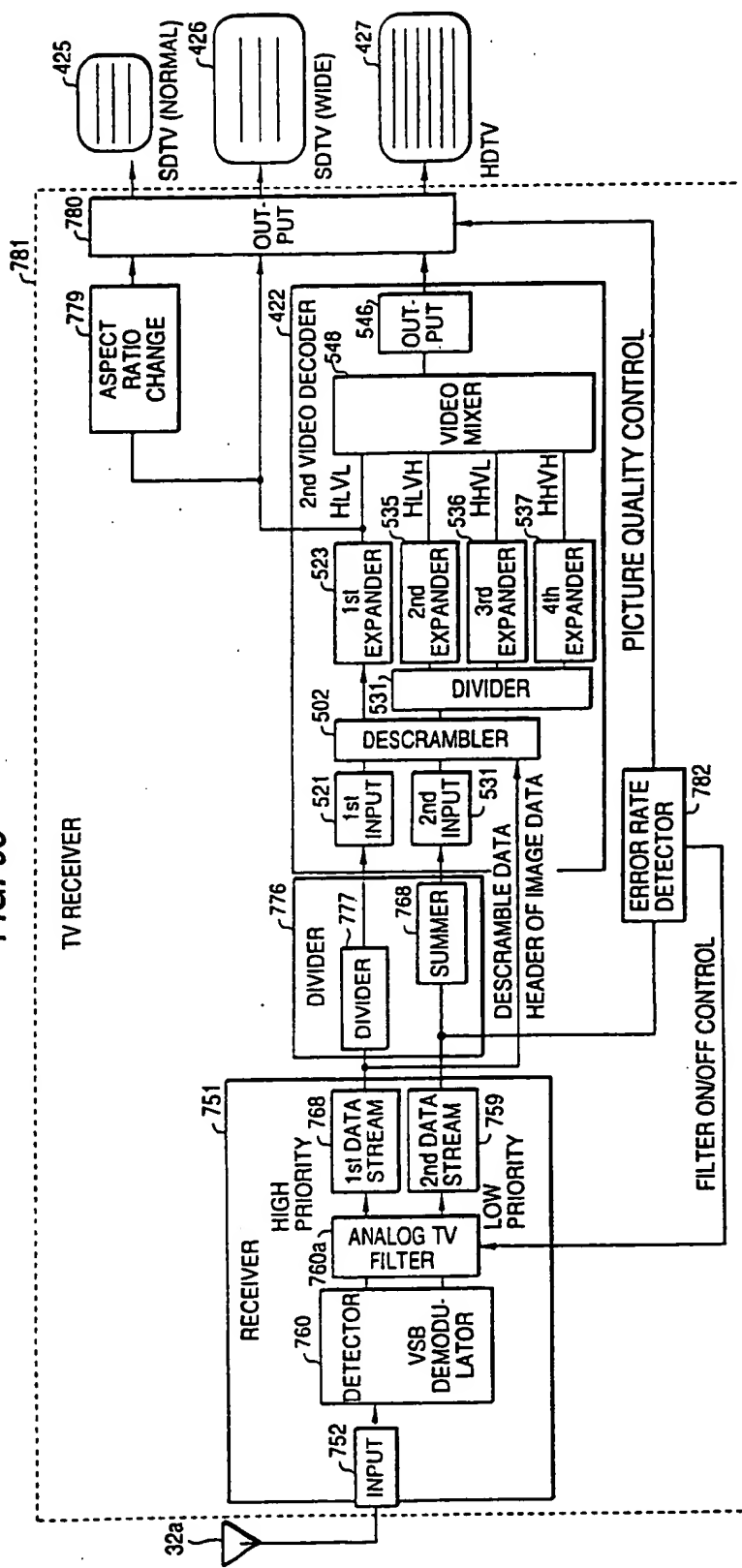


FIG. 66

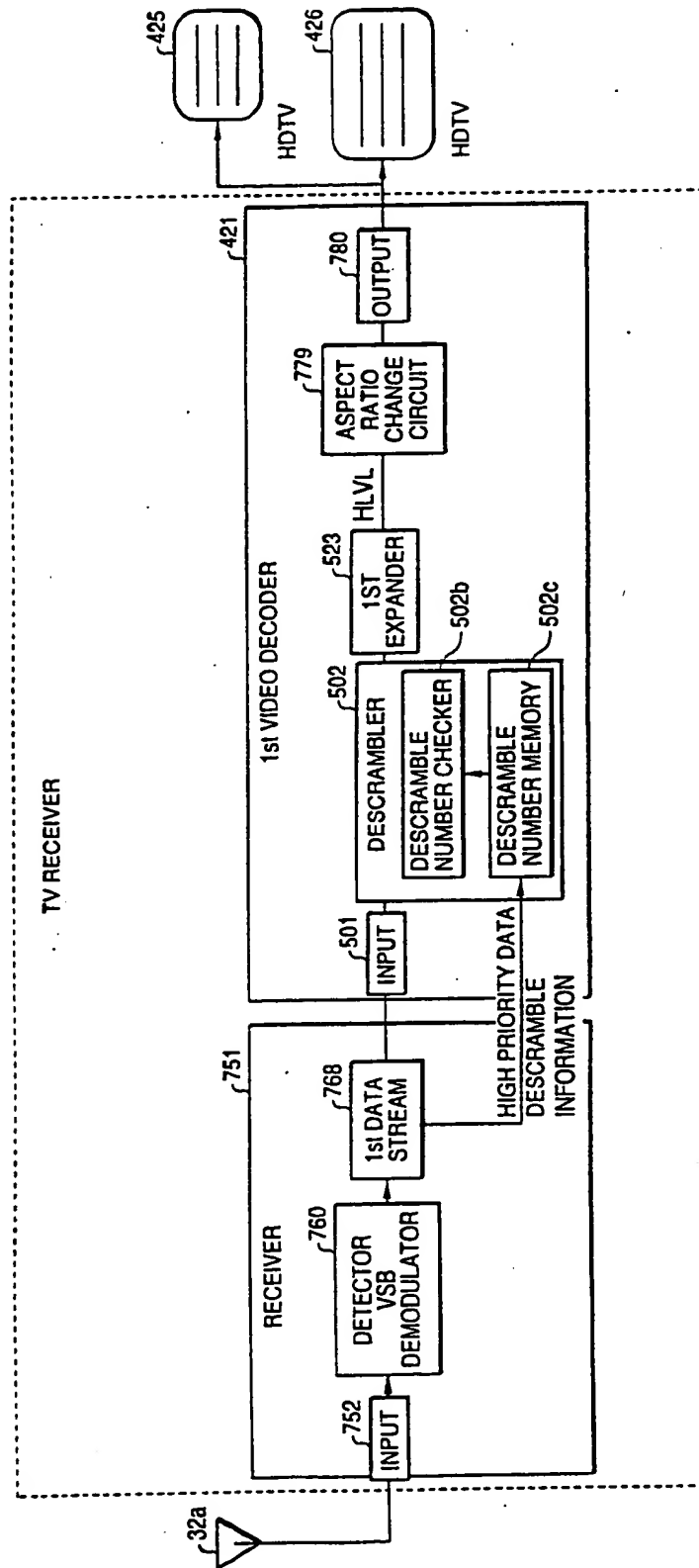
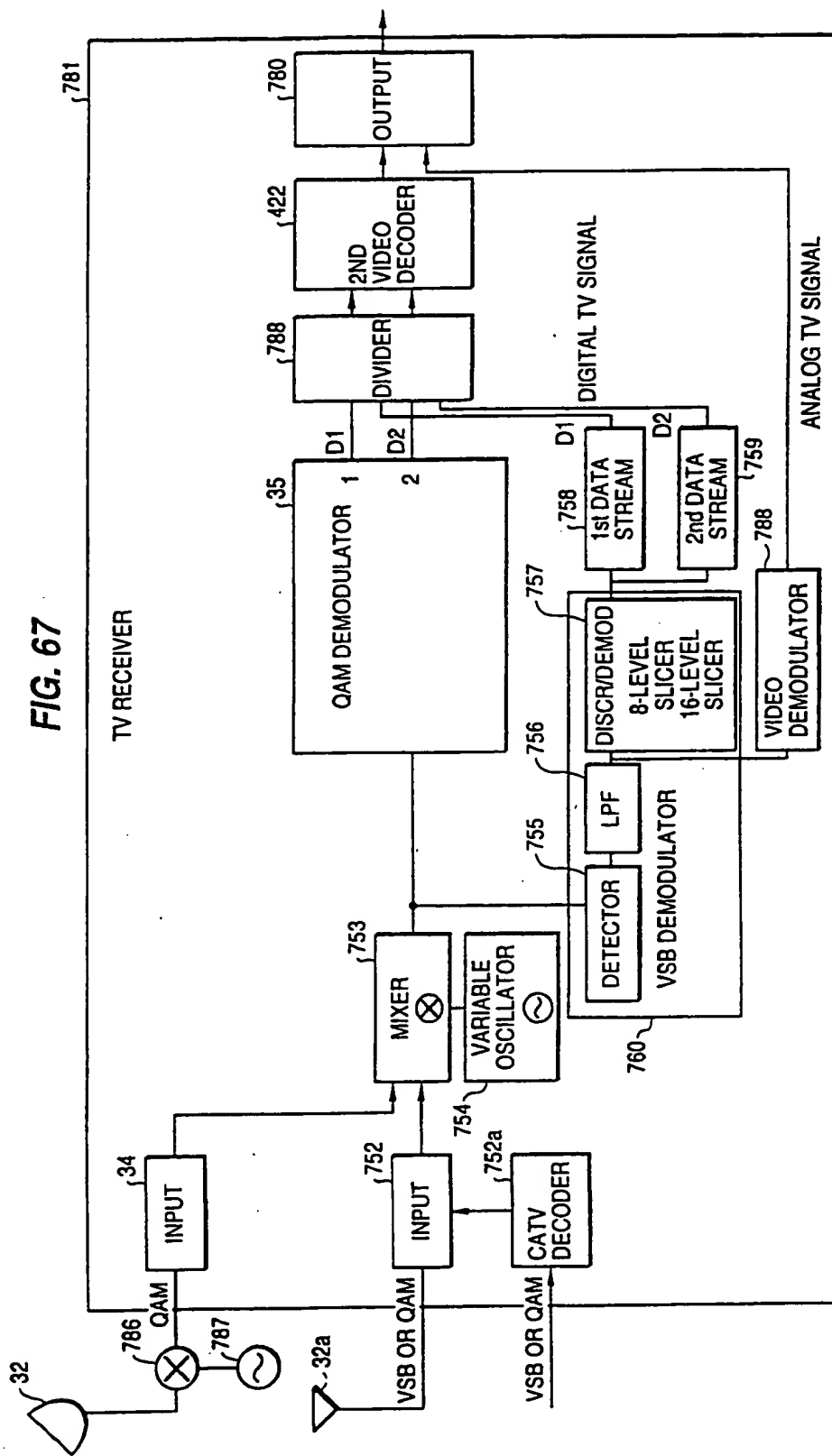


FIG. 67



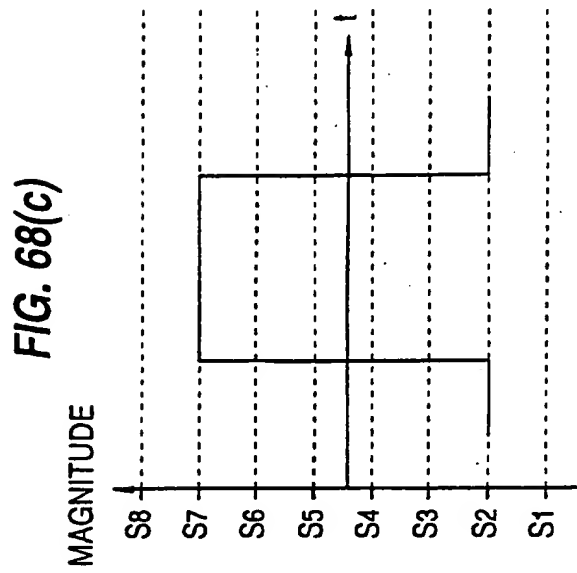
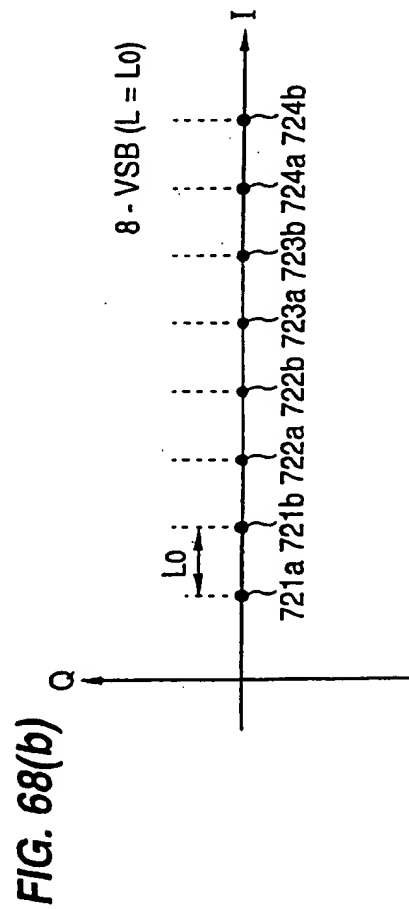
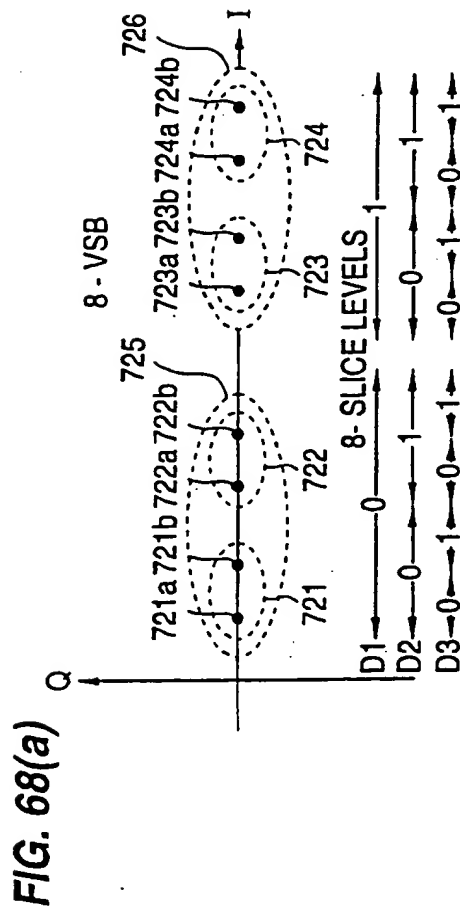


FIG. 69

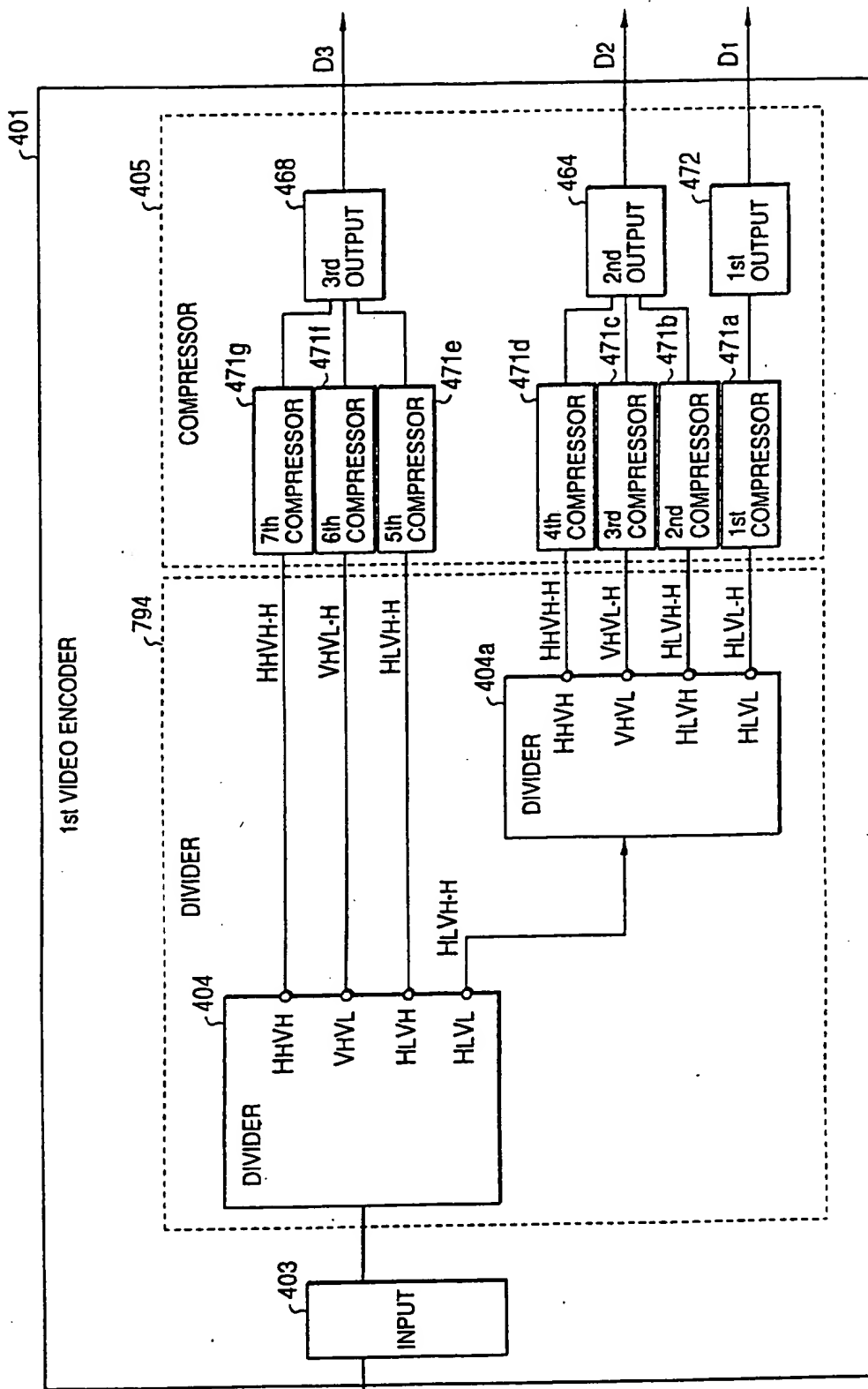


FIG. 70

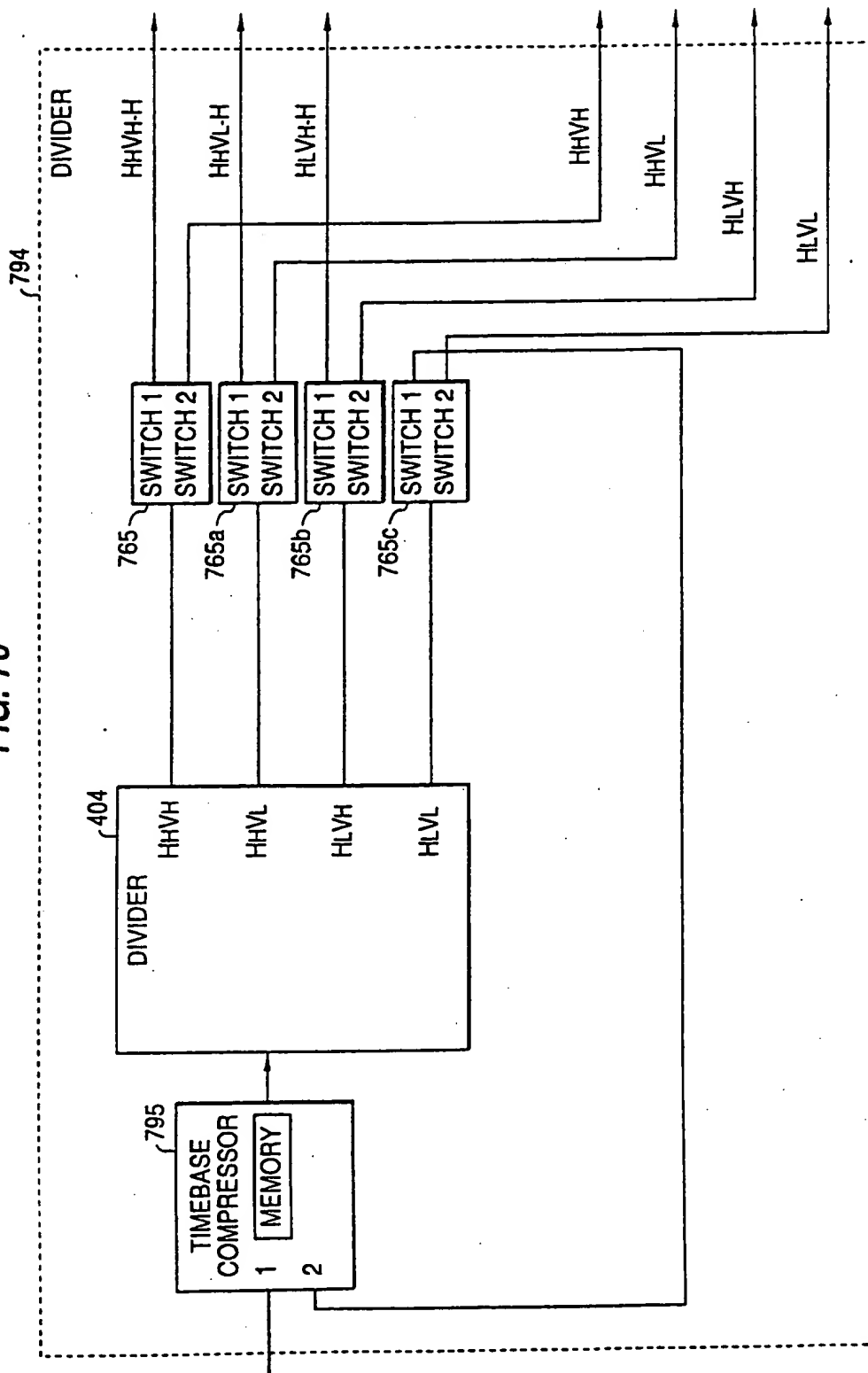


FIG. 71

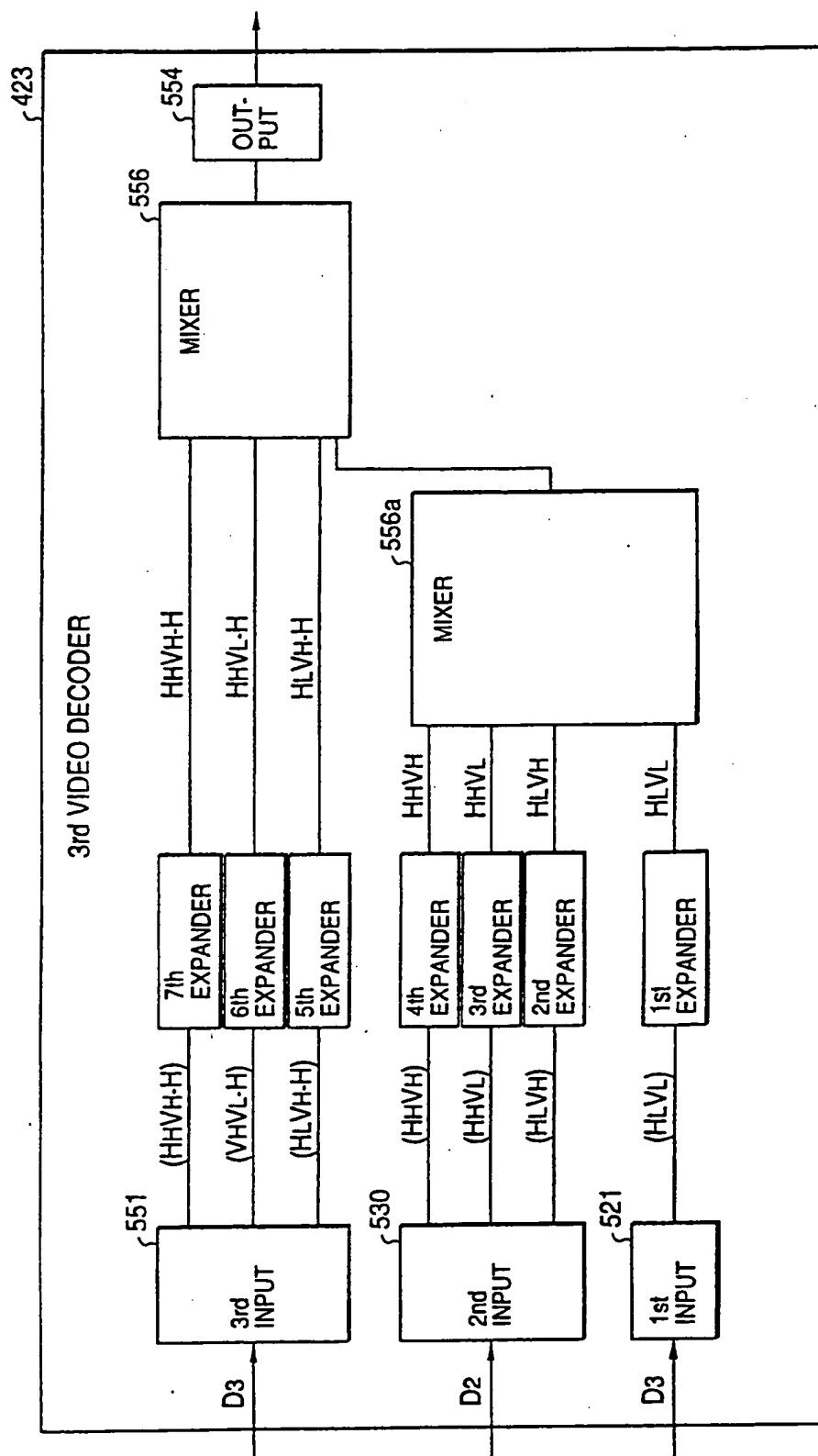


FIG. 72

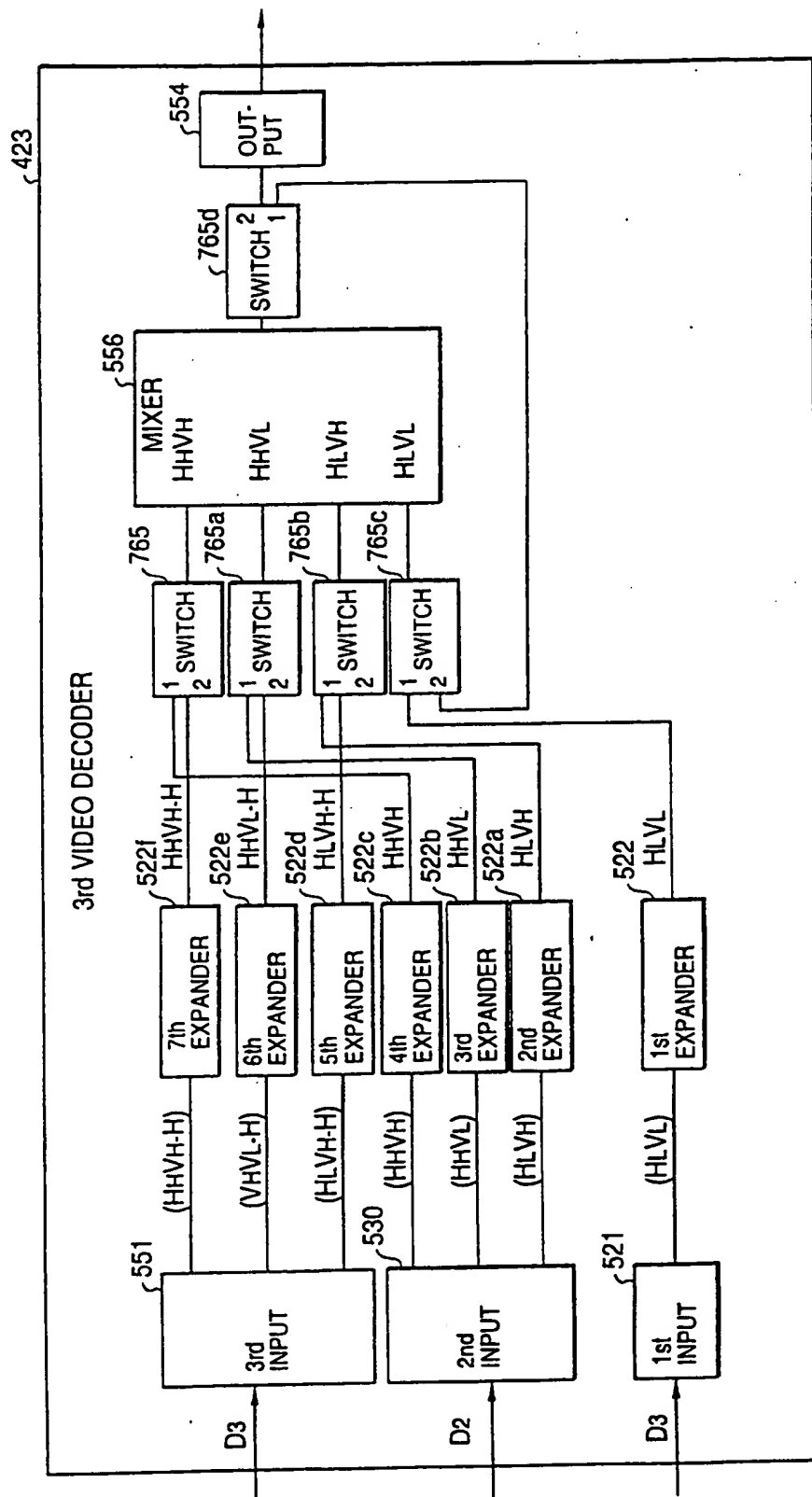


FIG. 73

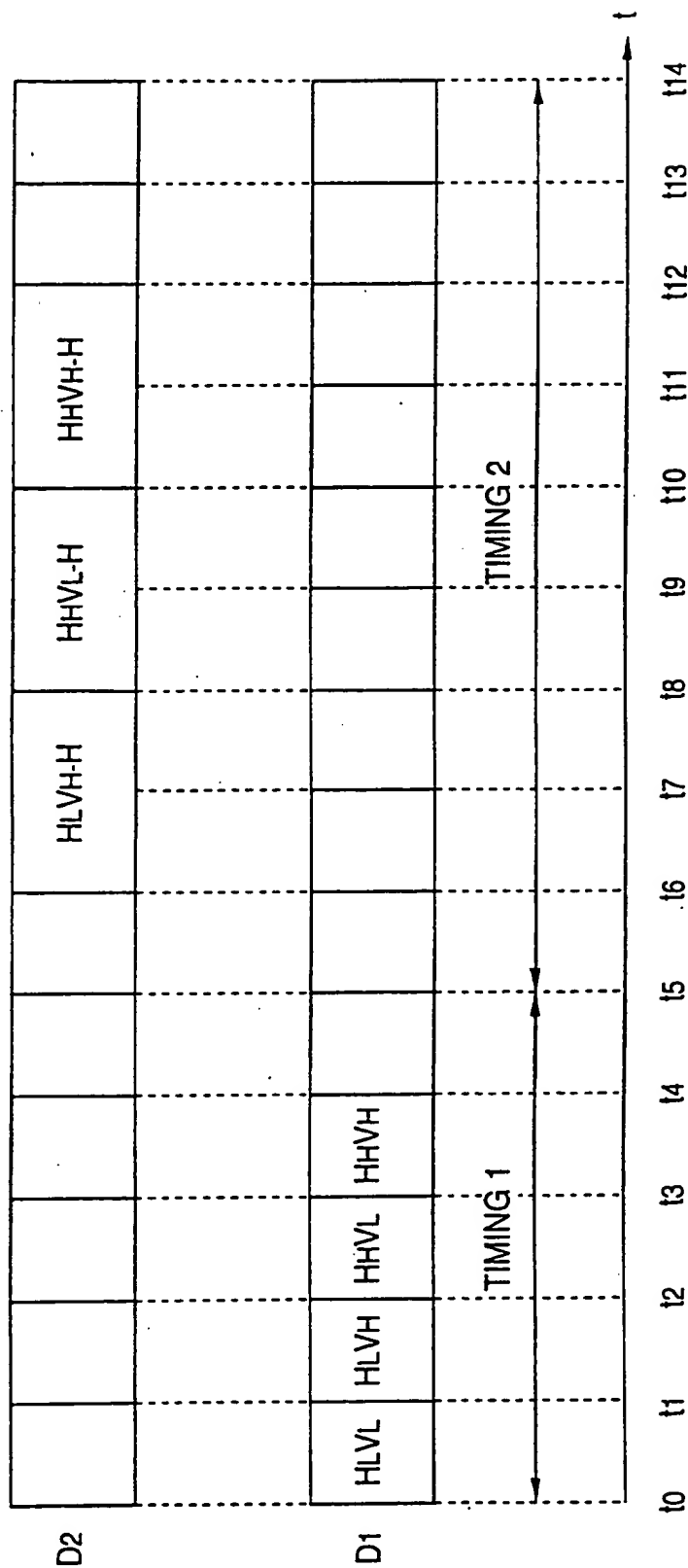


FIG. 74(a)

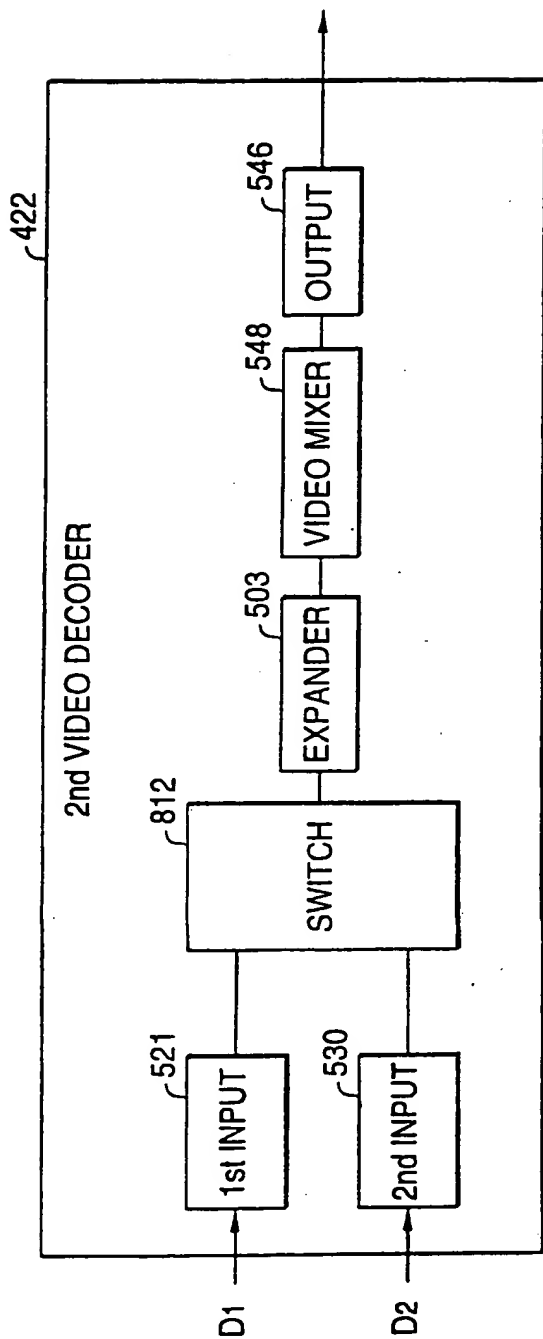


FIG. 74(b)

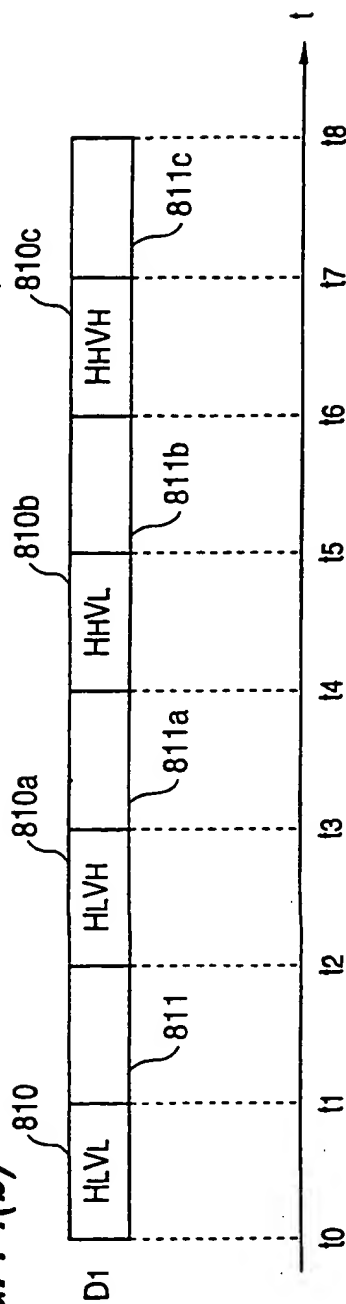




FIG. 76

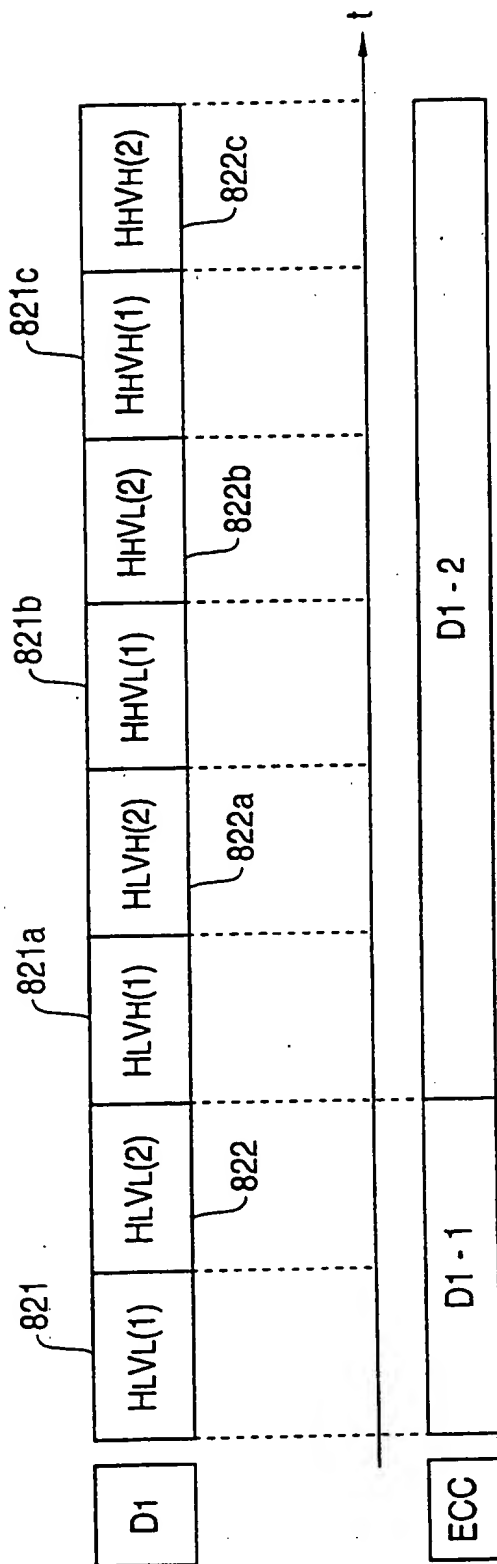


FIG. 77

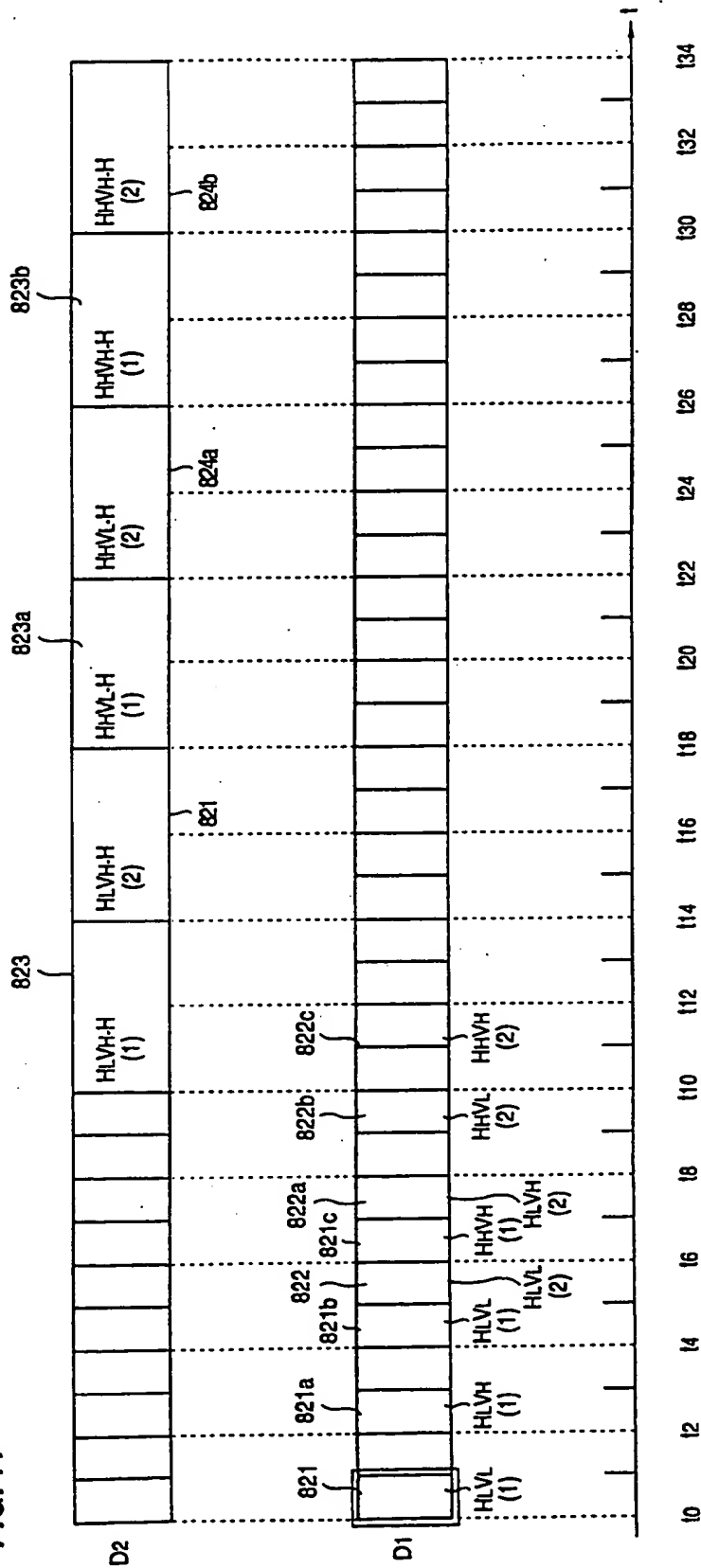
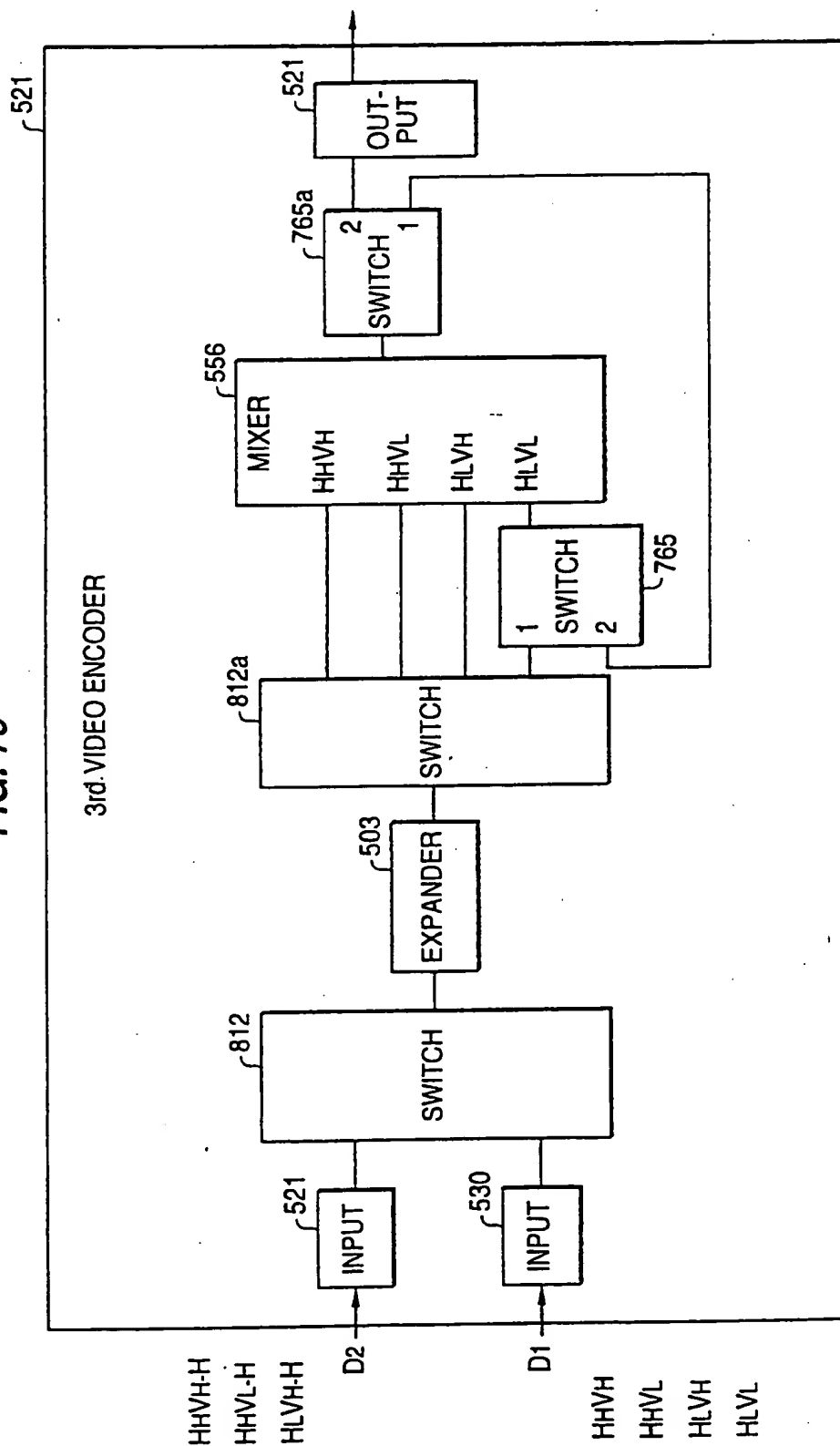


FIG. 78



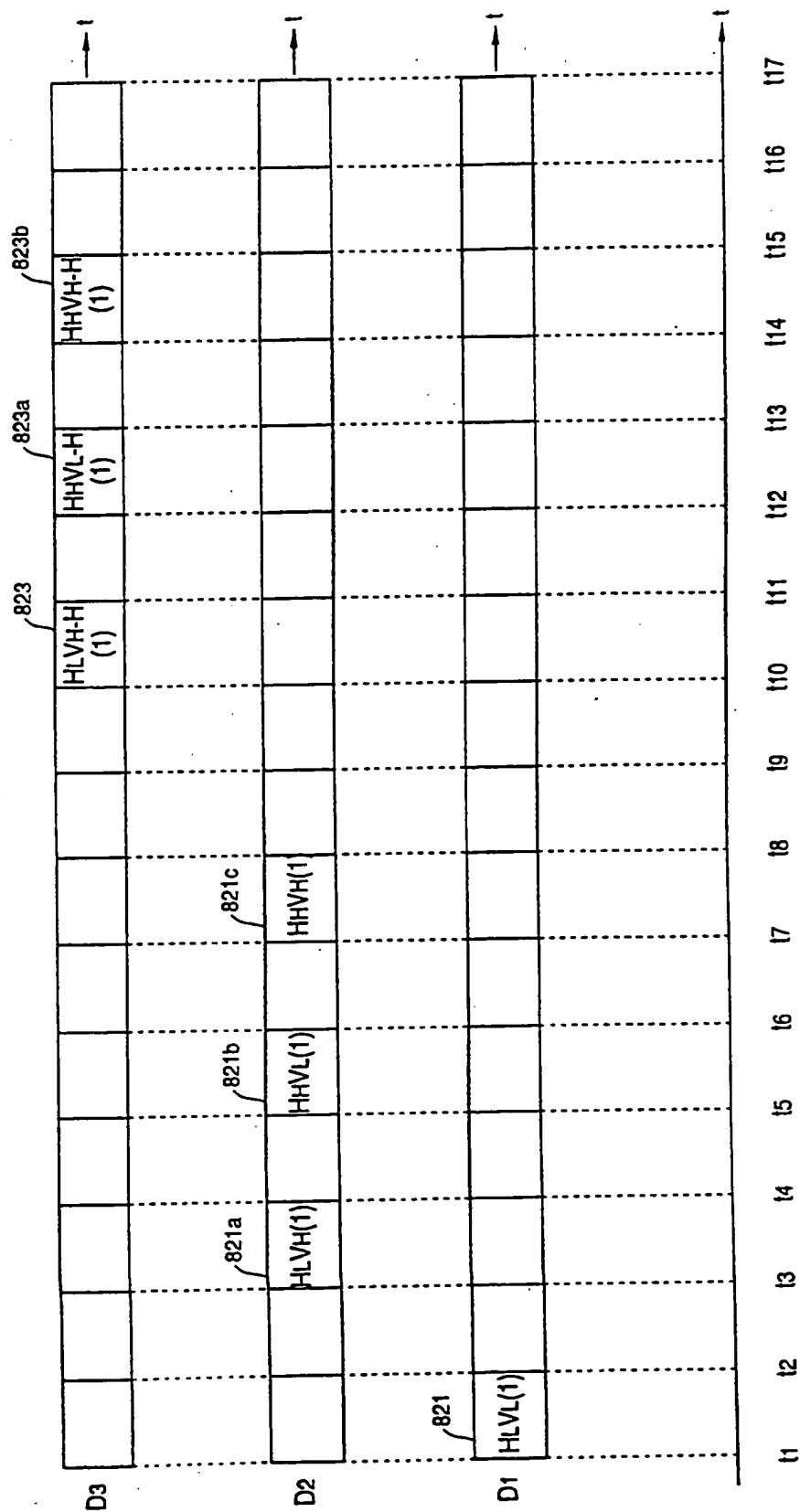


FIG. 80

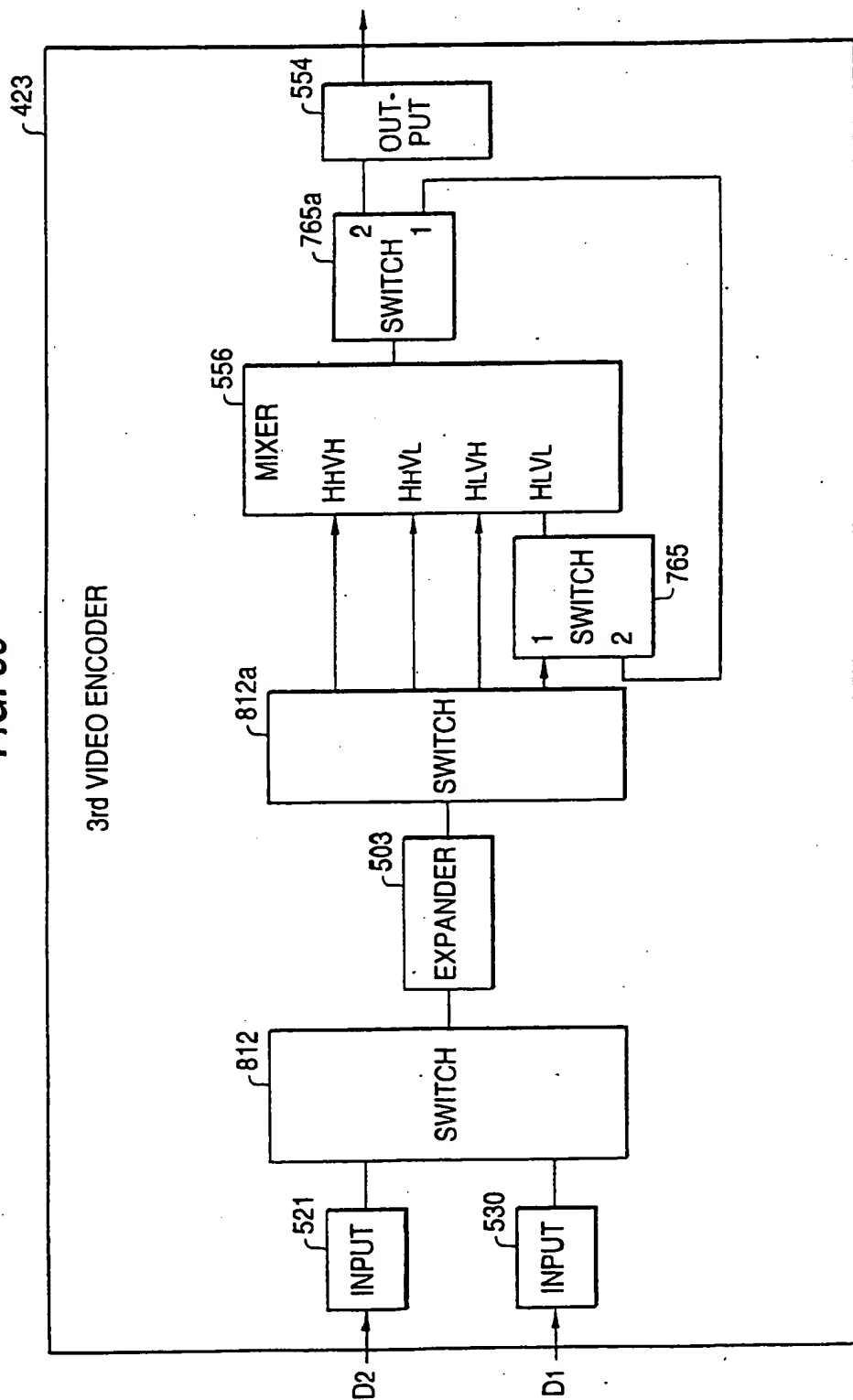
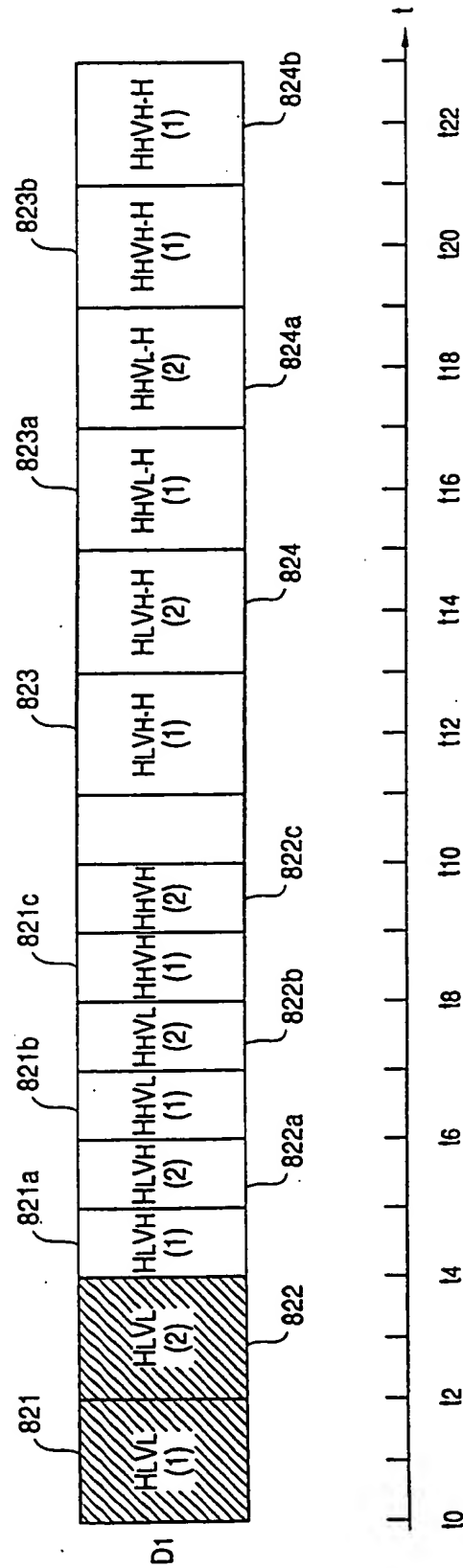


FIG. 81



000007 4703350

FIG. 82

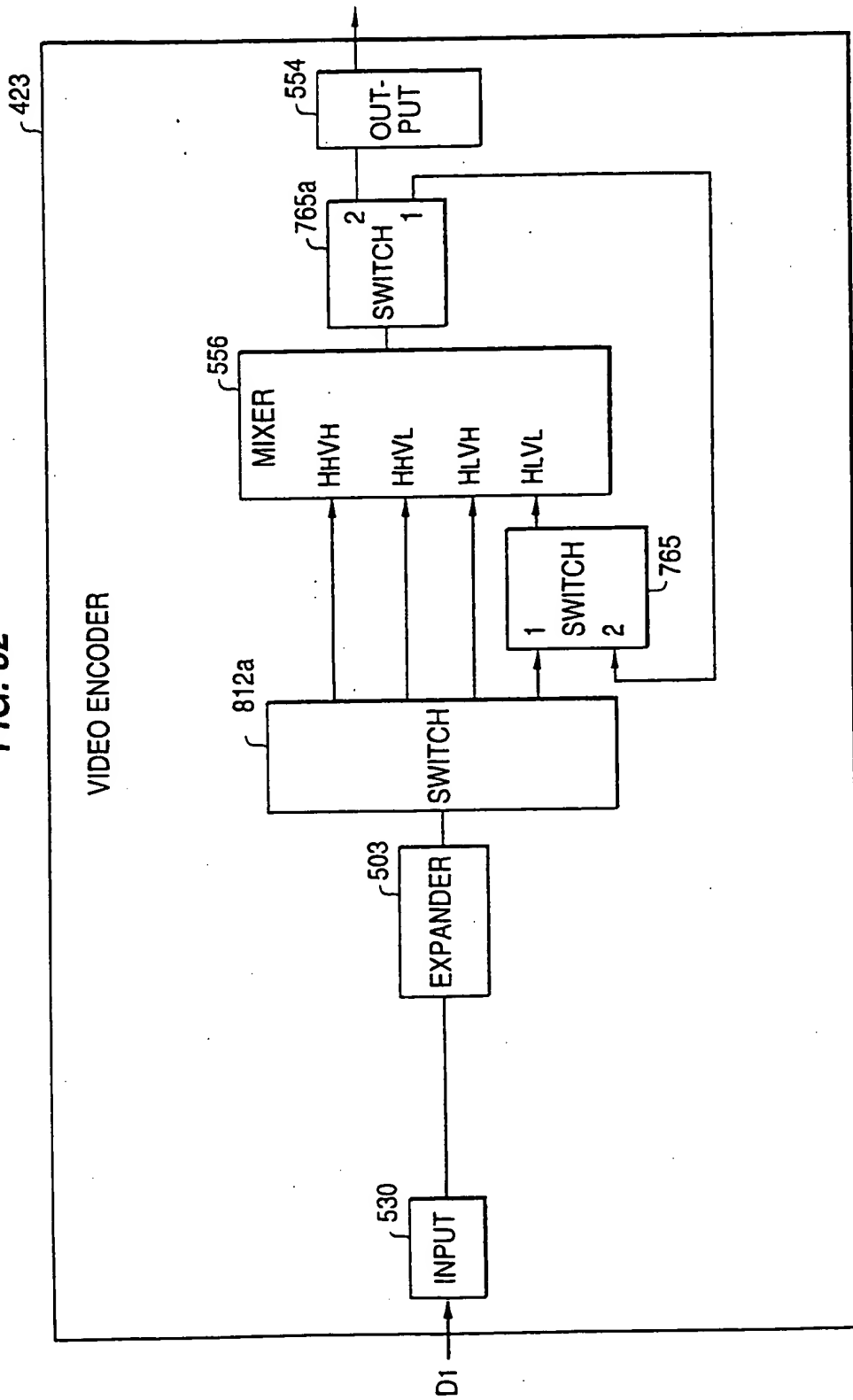


FIG. 83

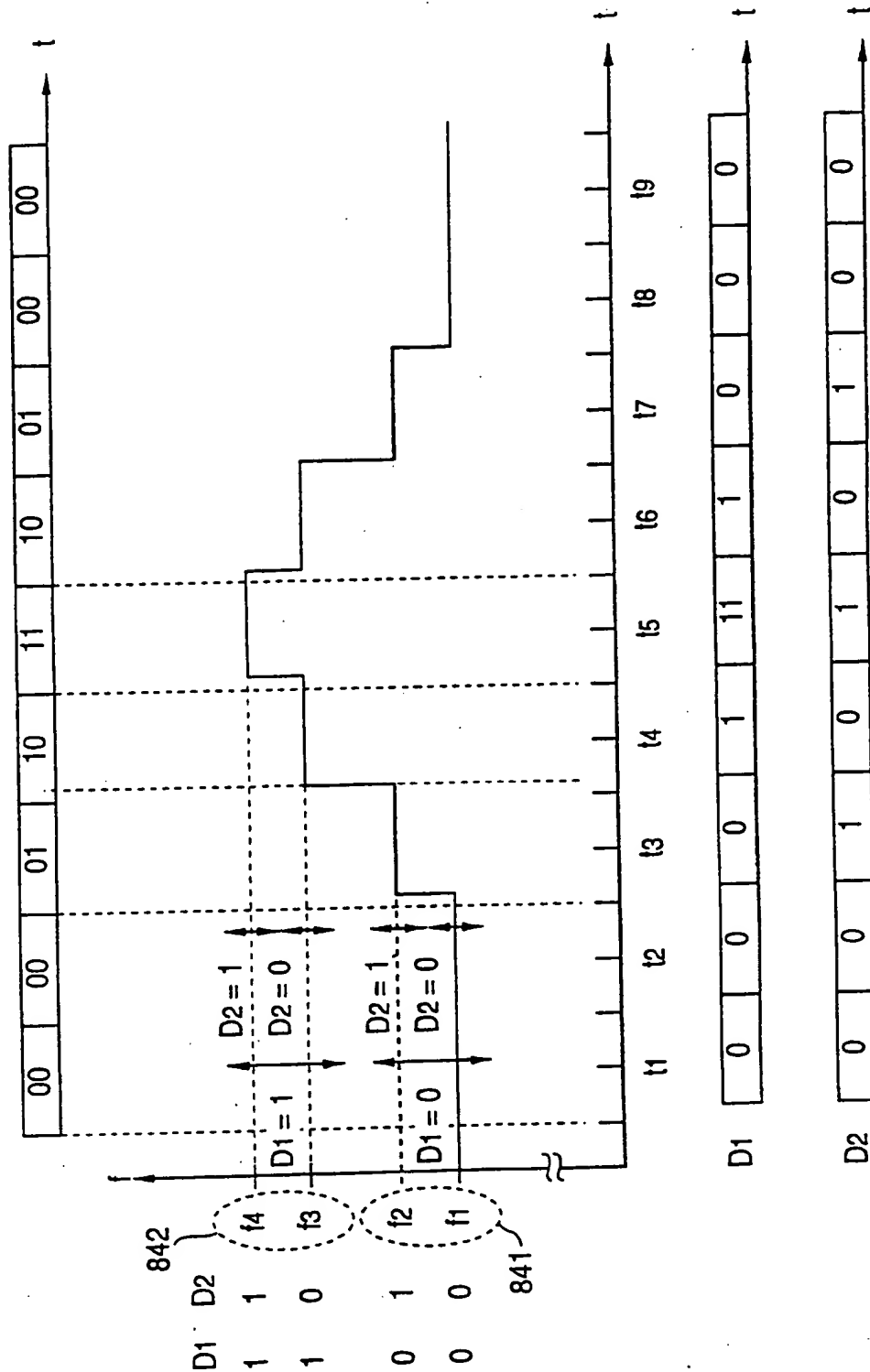


FIG. 84

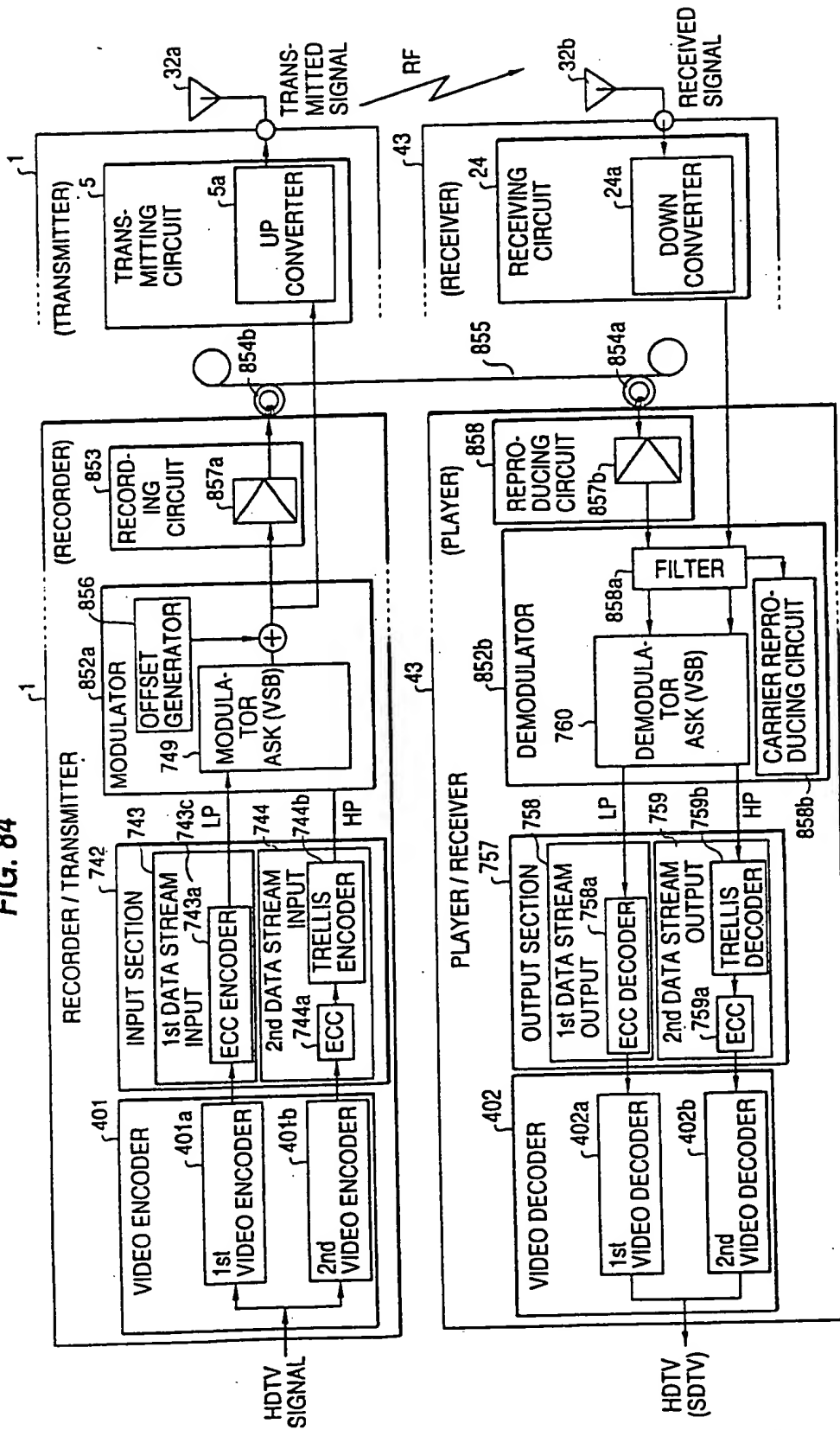


FIG. 85

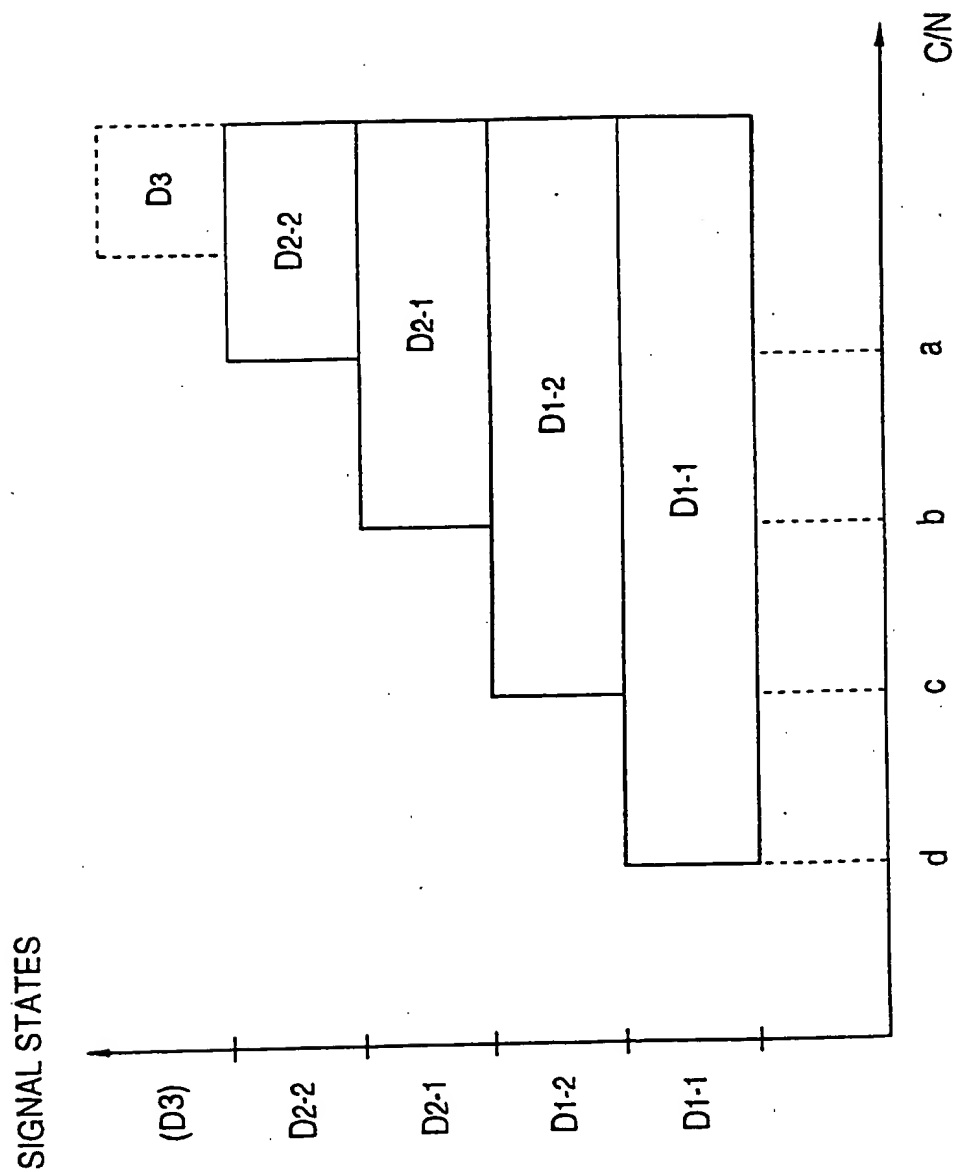
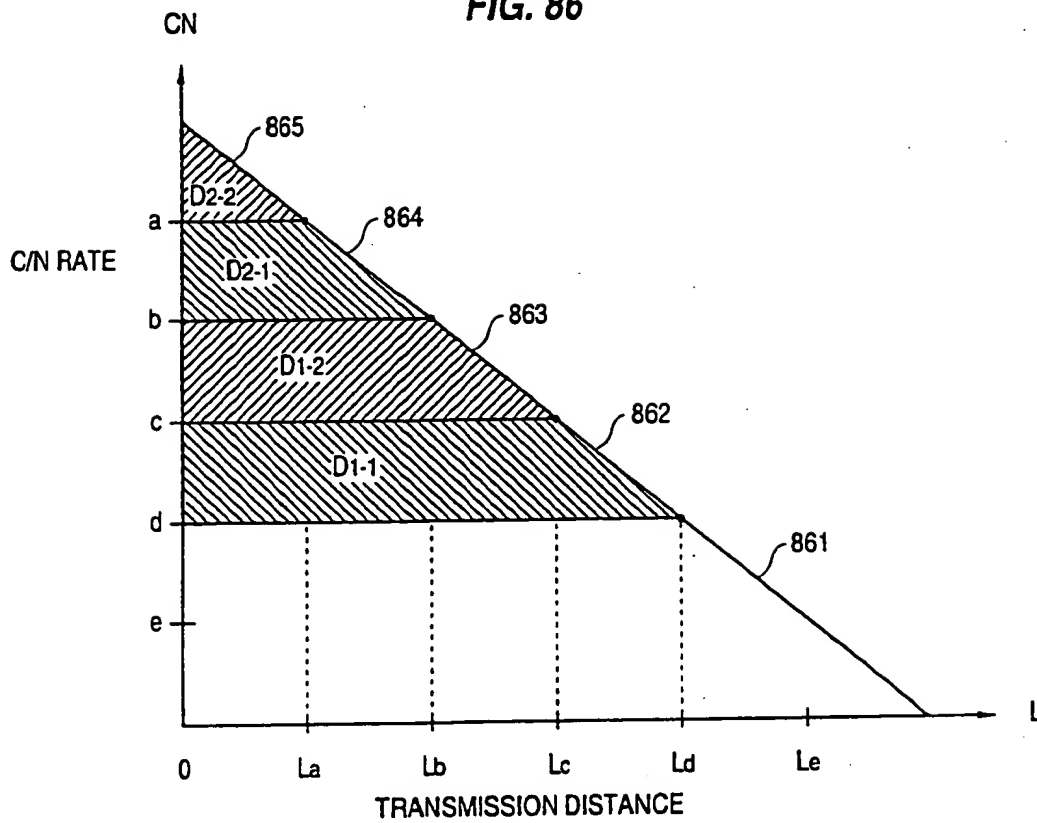
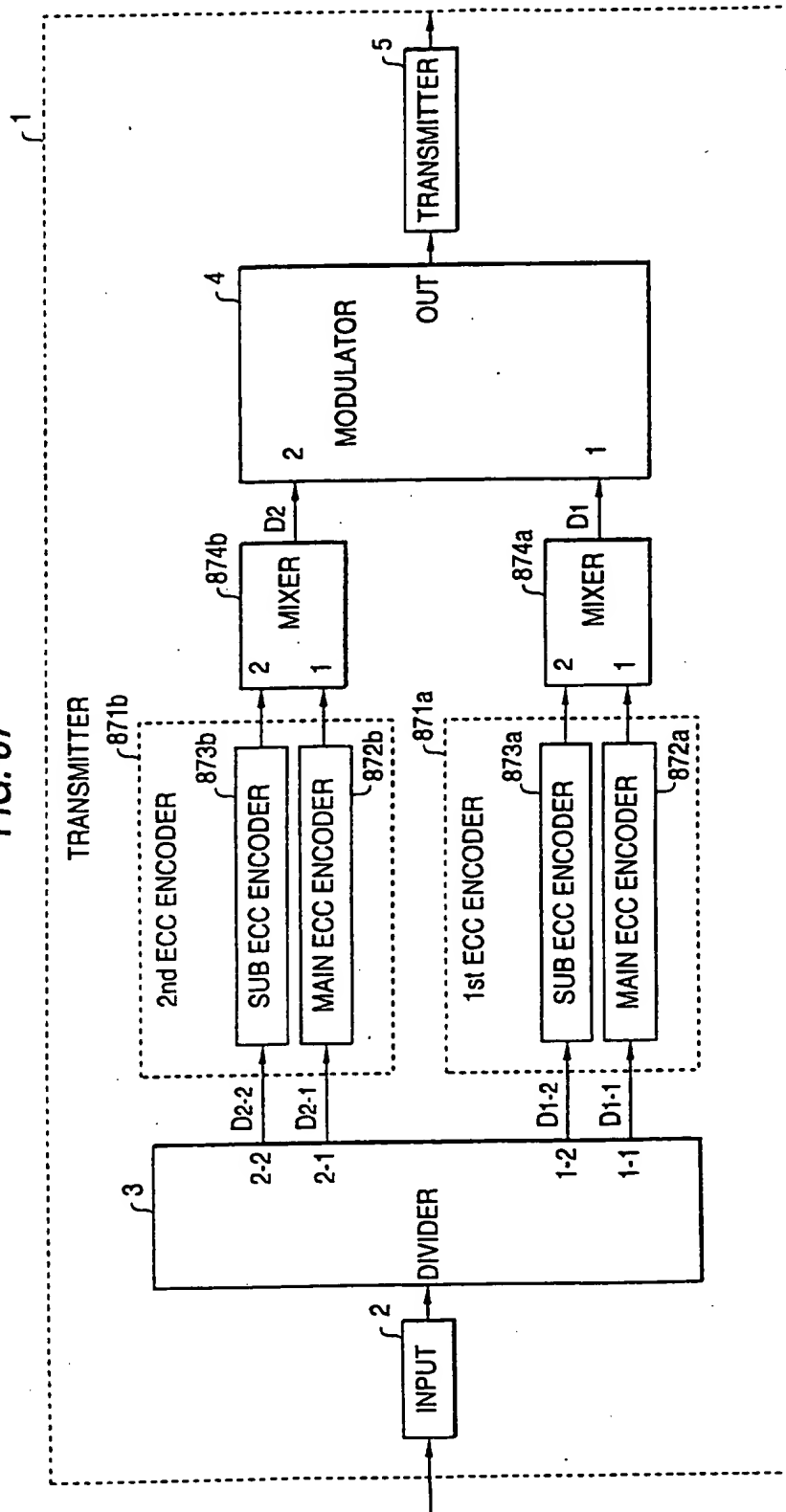


FIG. 86



09660177-1006000

FIG. 87



005001/2409960

FIG. 88

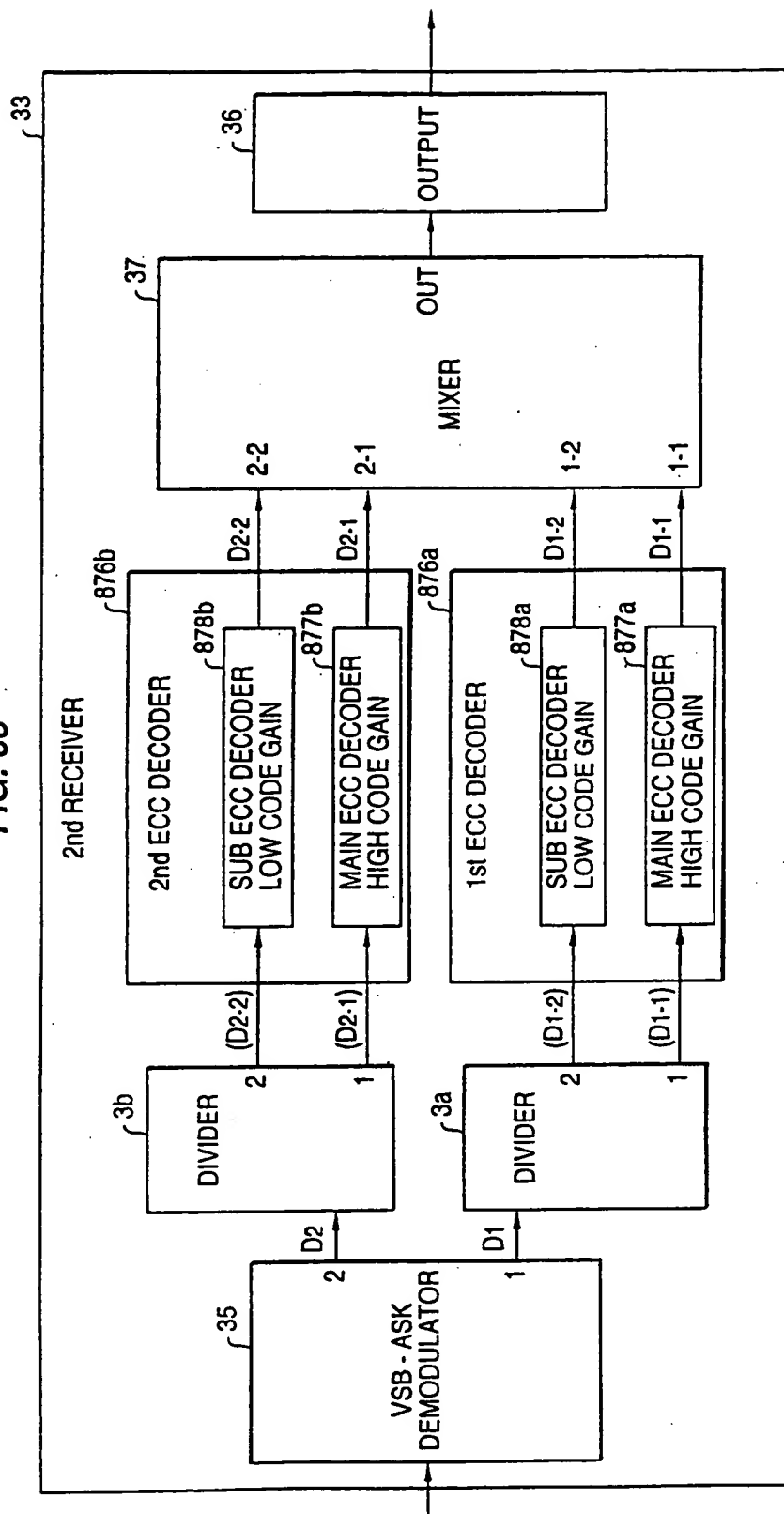
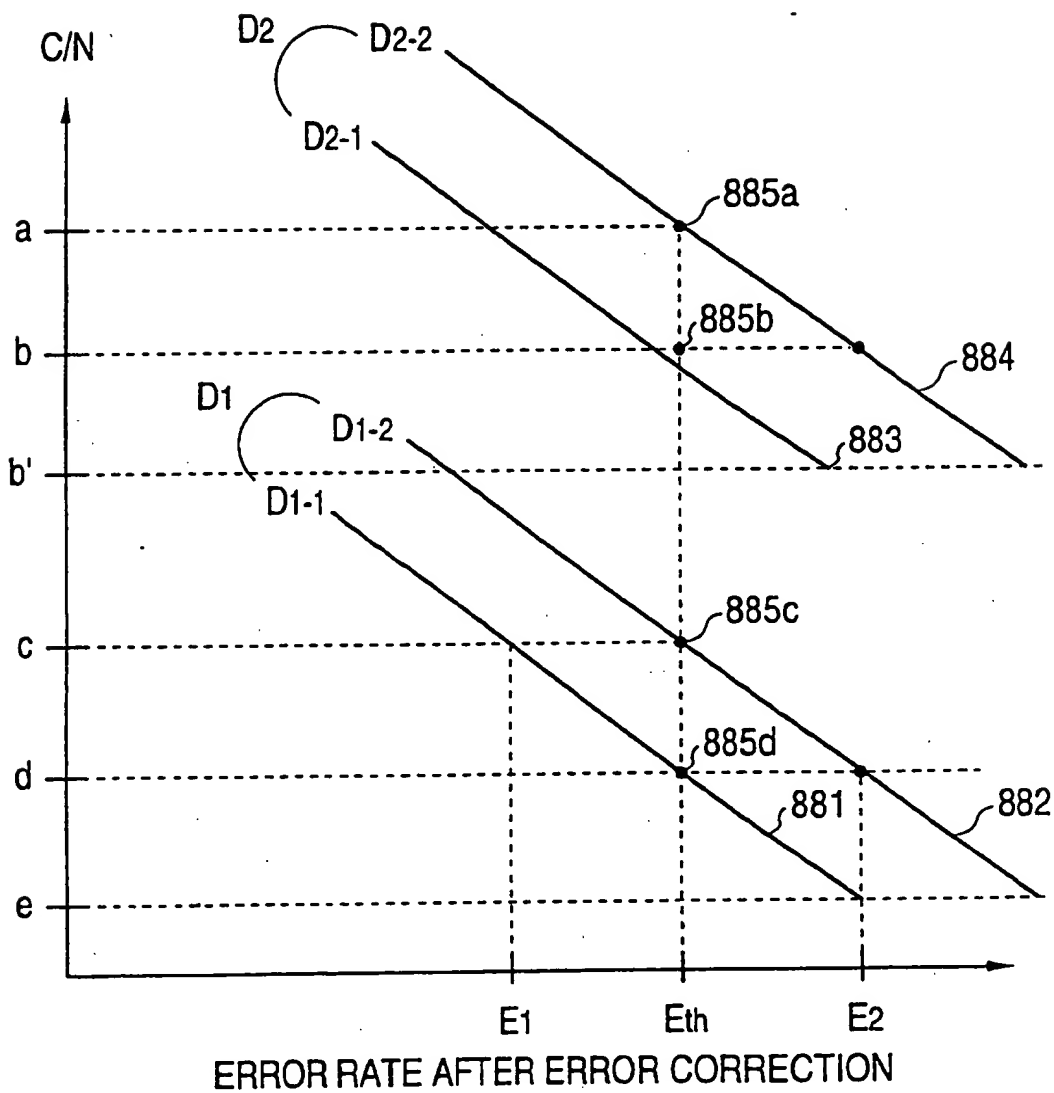


FIG. 89



00500T/2703950

FIG. 90

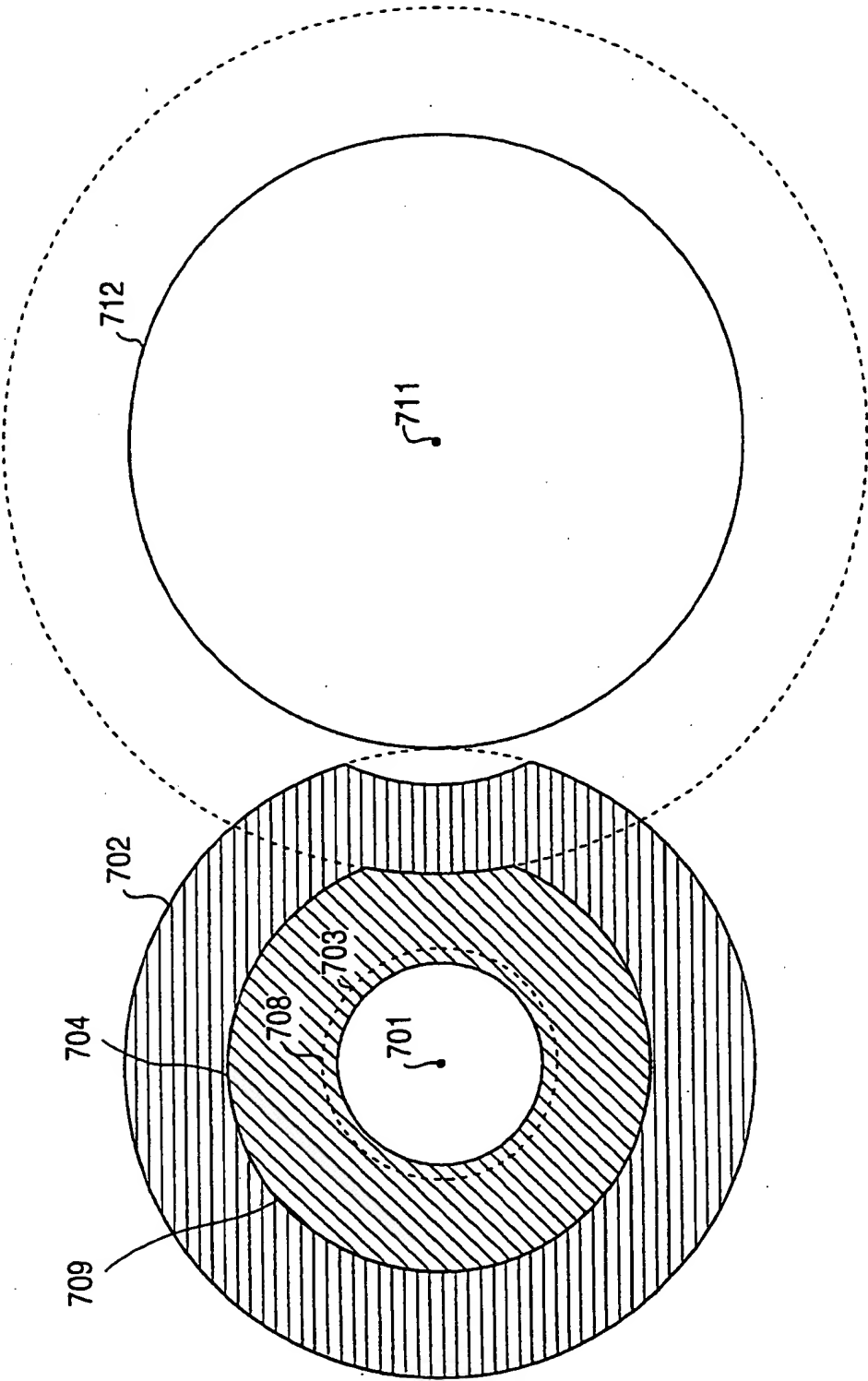
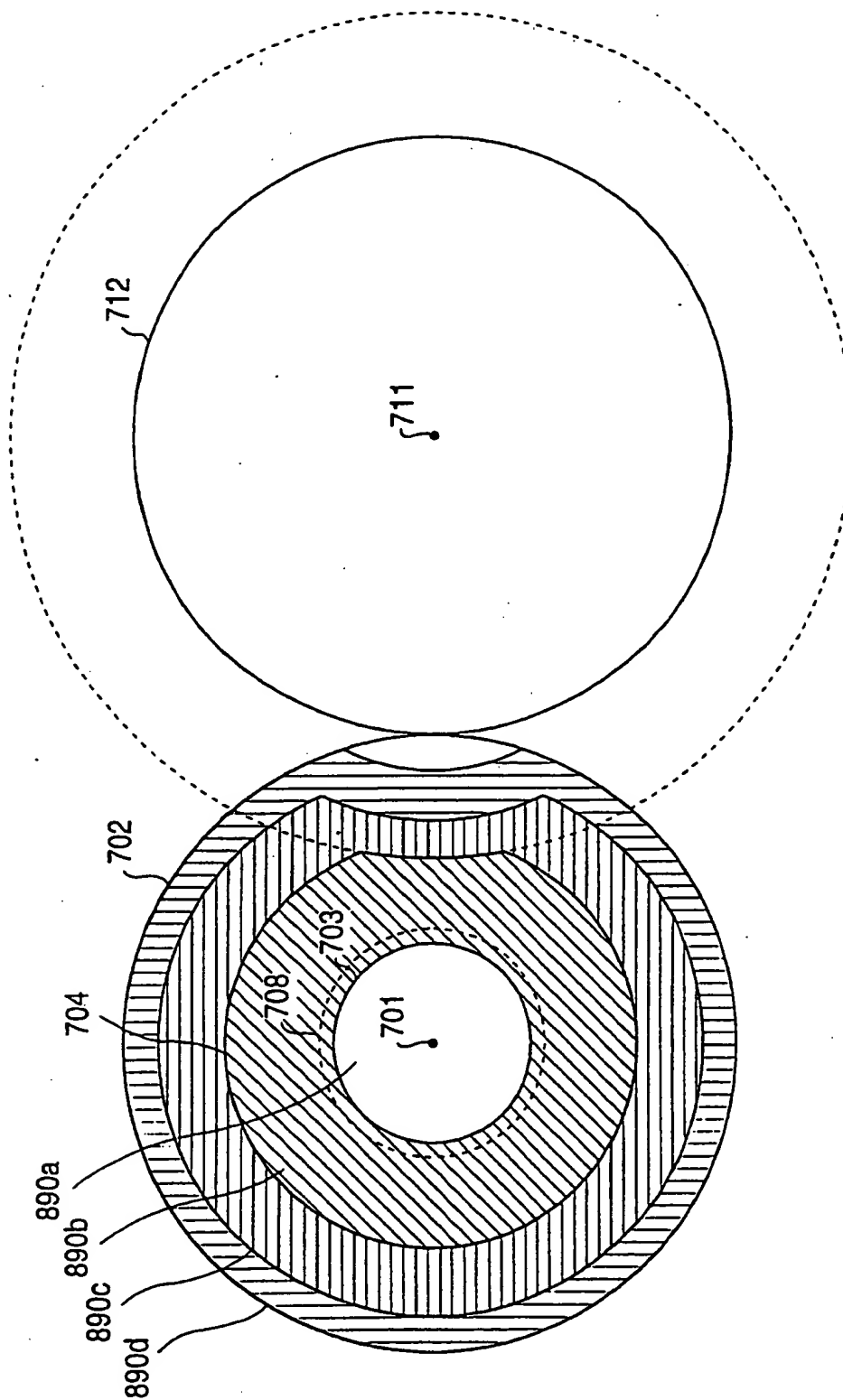


FIG. 91



000007 4703360

FIG. 92

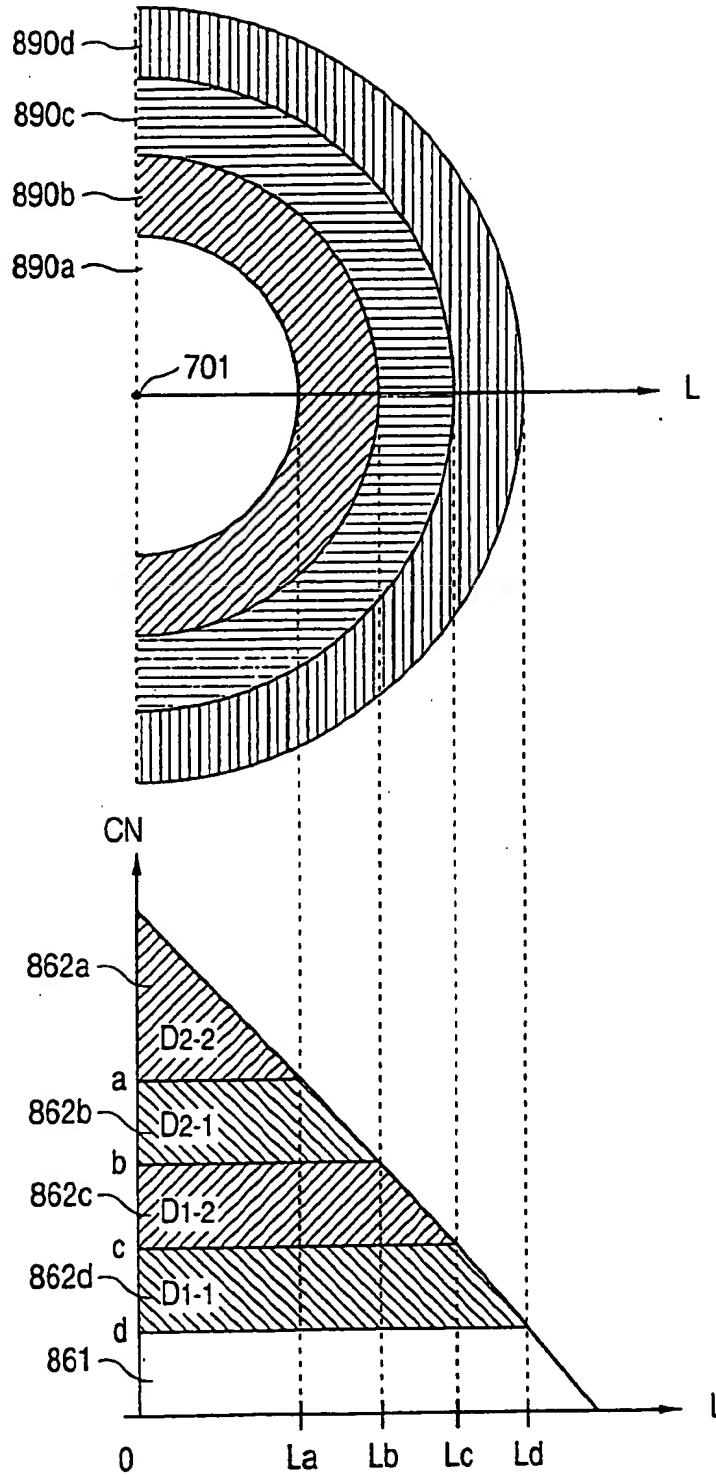
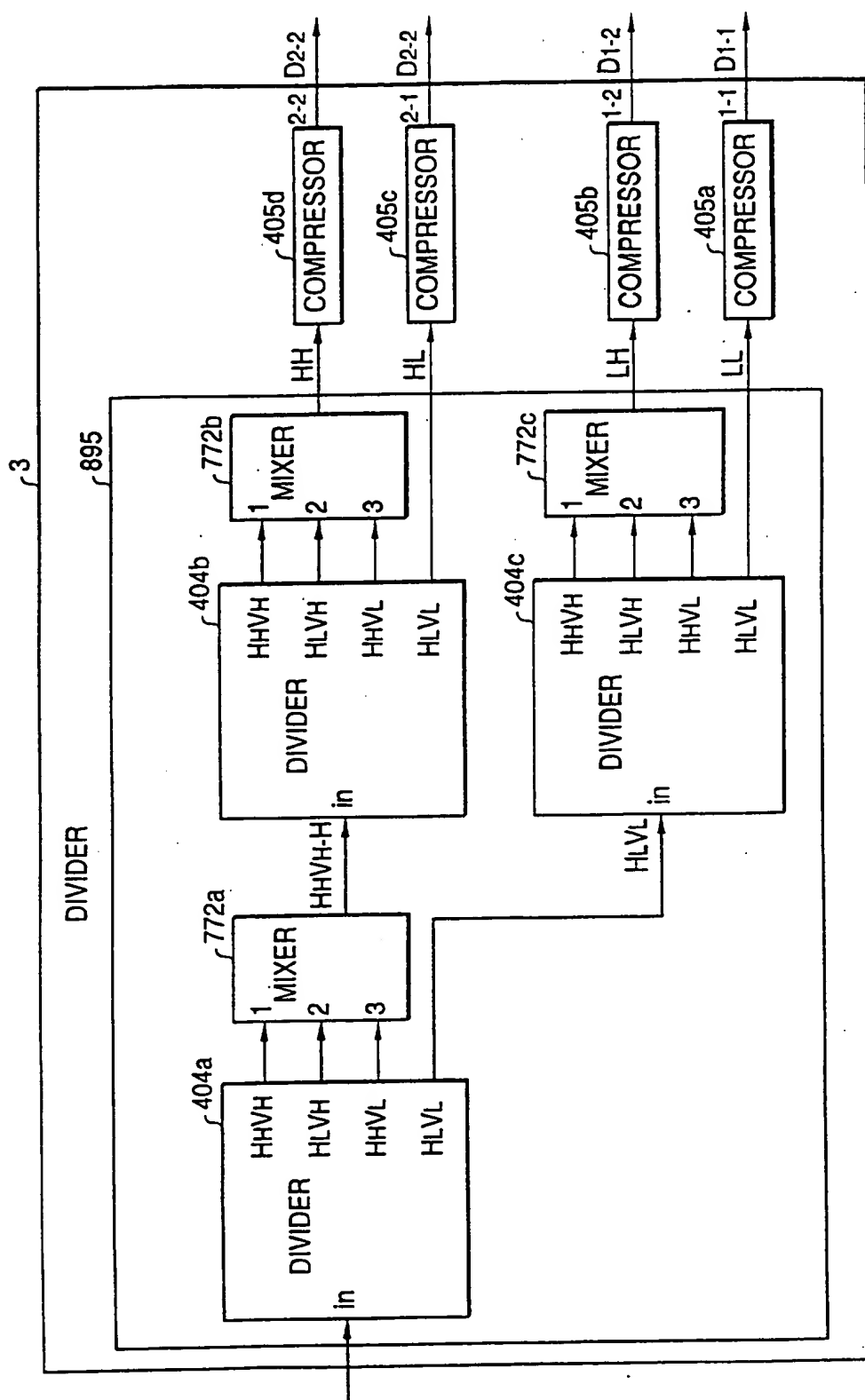


FIG. 93



005007 2/29/96

FIG. 94

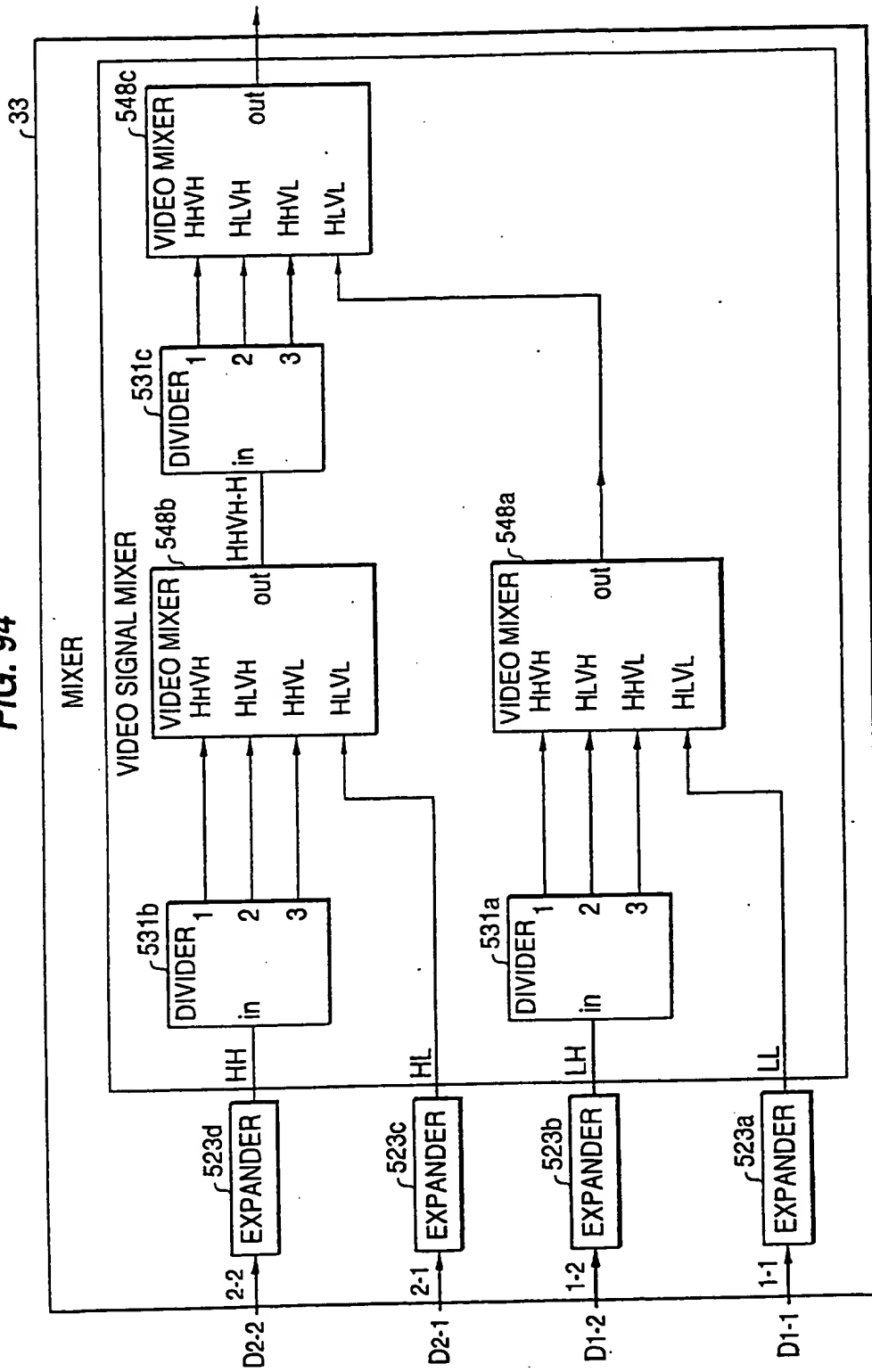


FIG. 95

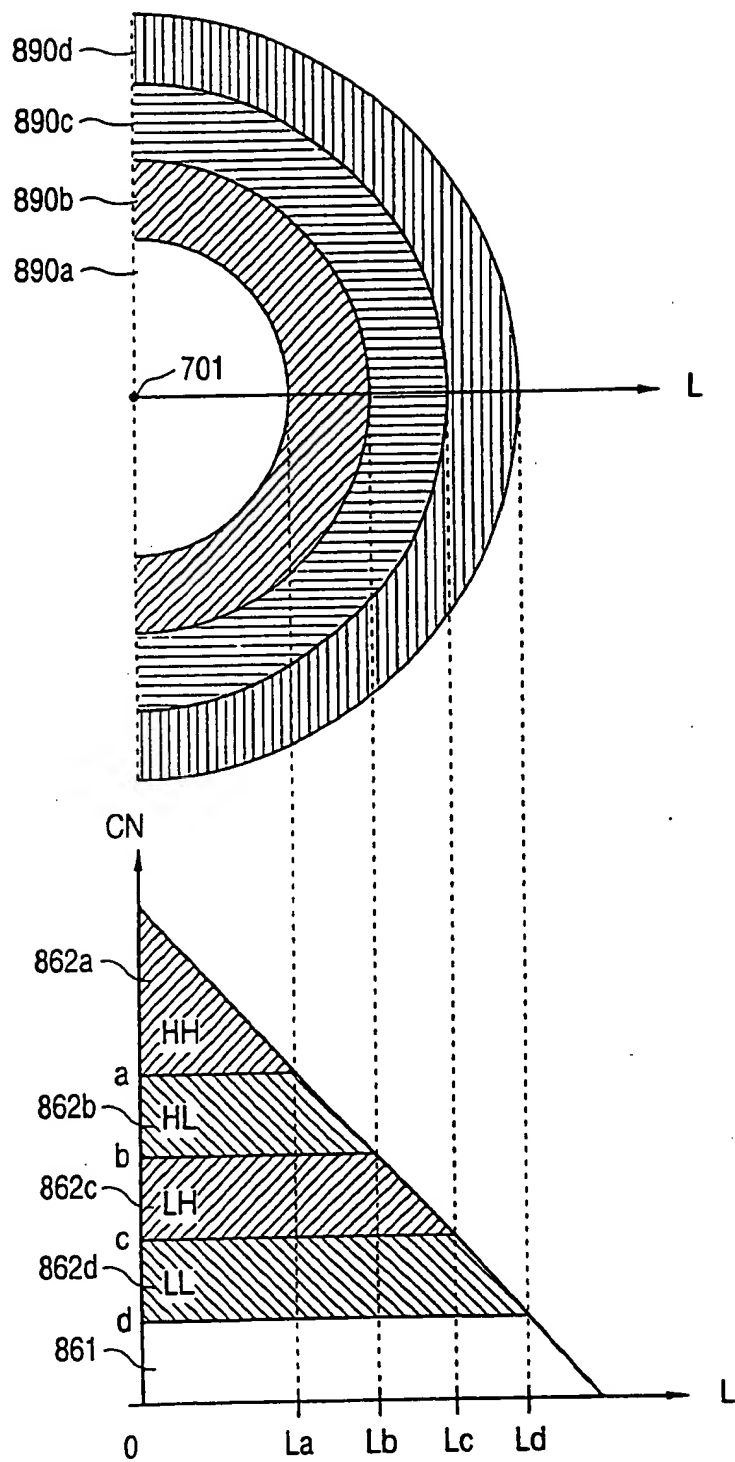


FIG. 96

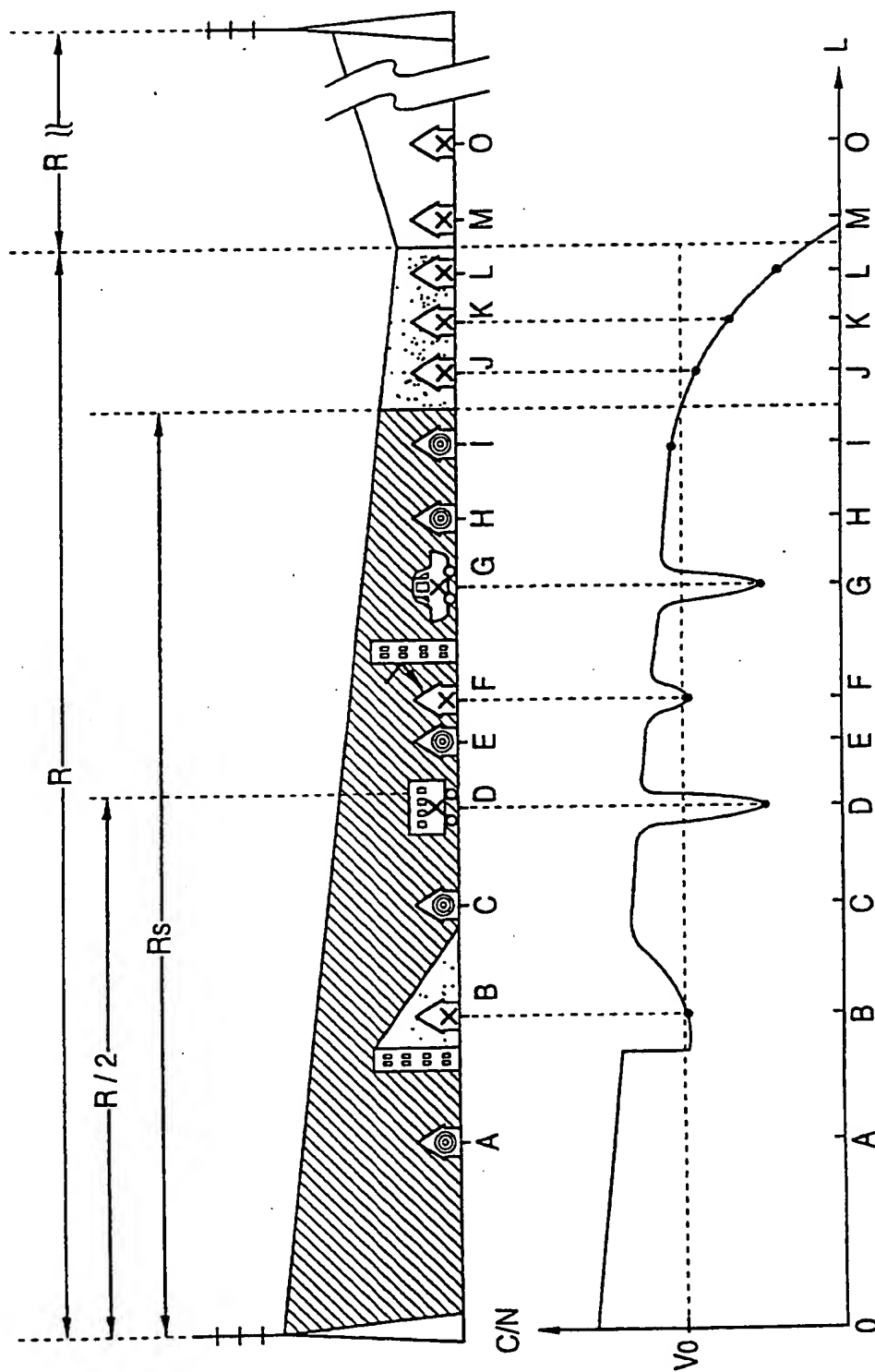


FIG. 97

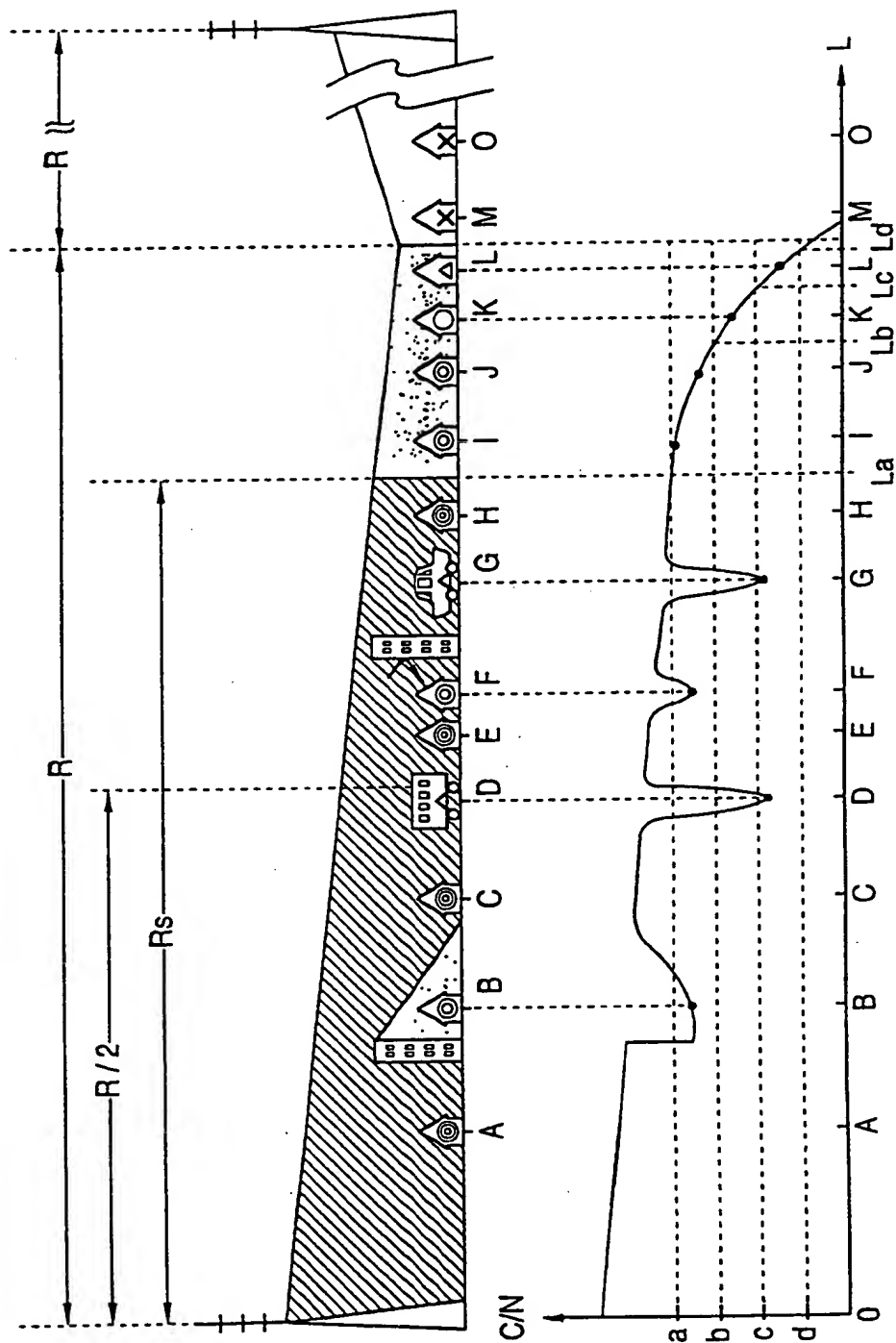


FIG. 98

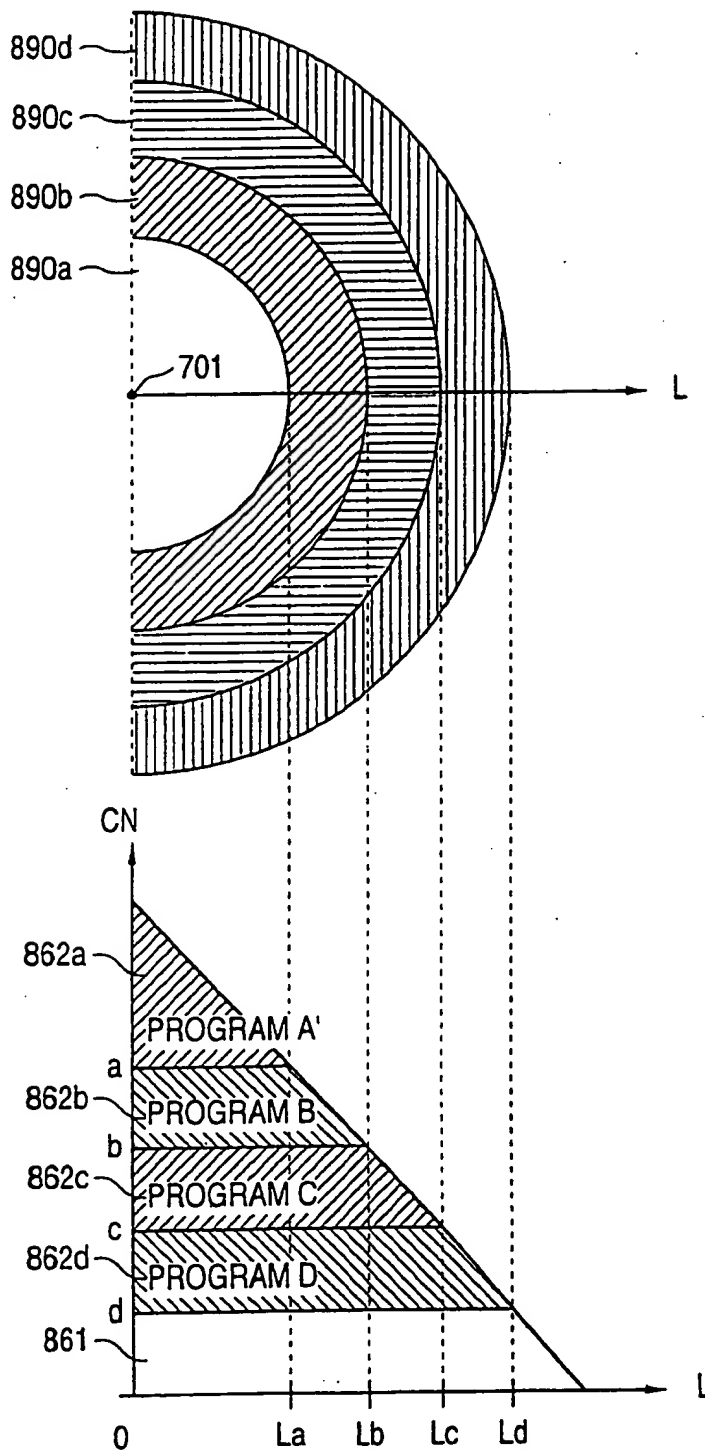


FIG. 99

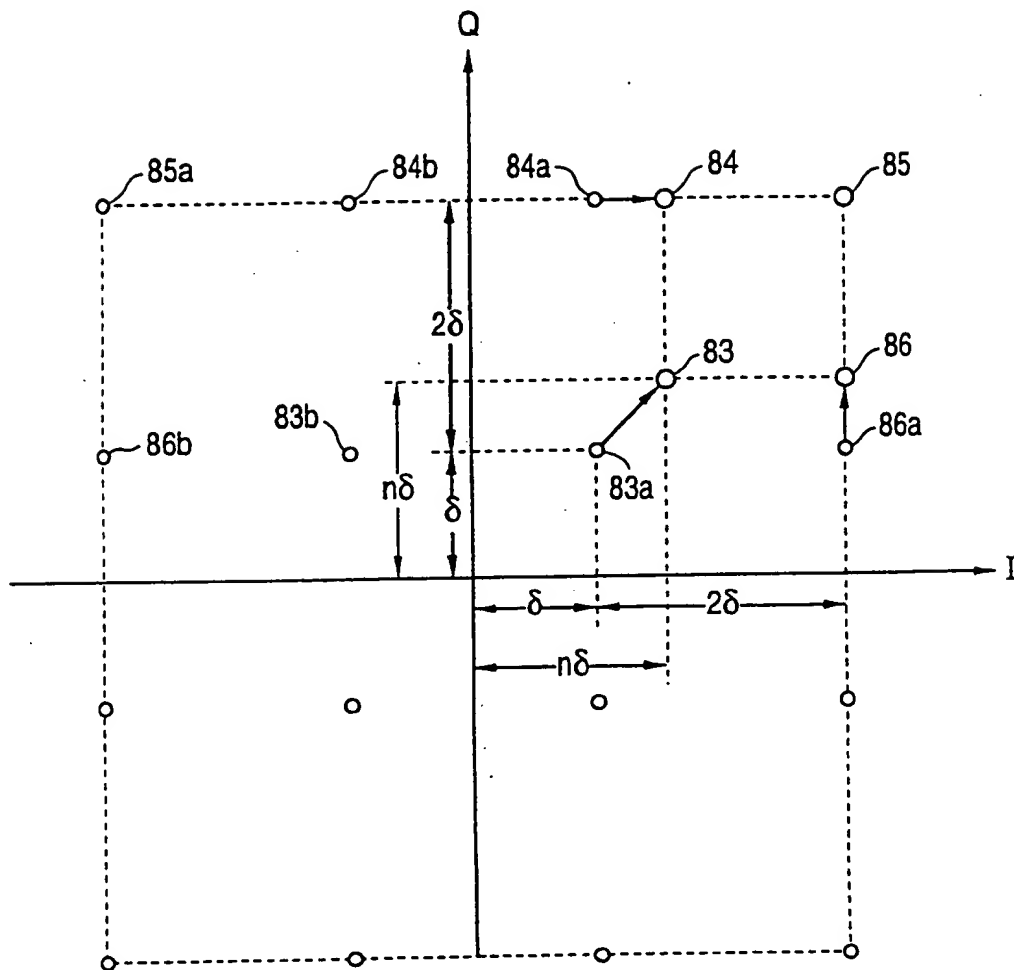


FIG. 100

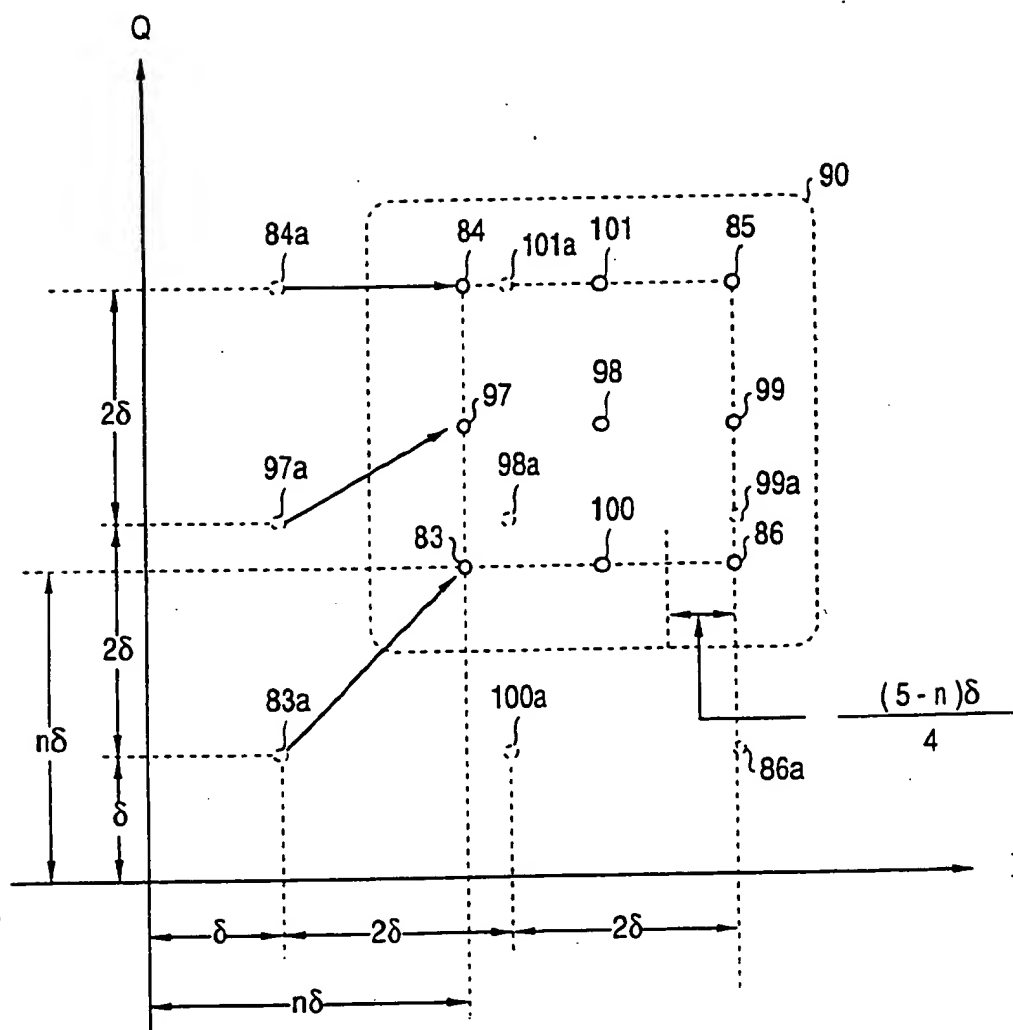


FIG. 101

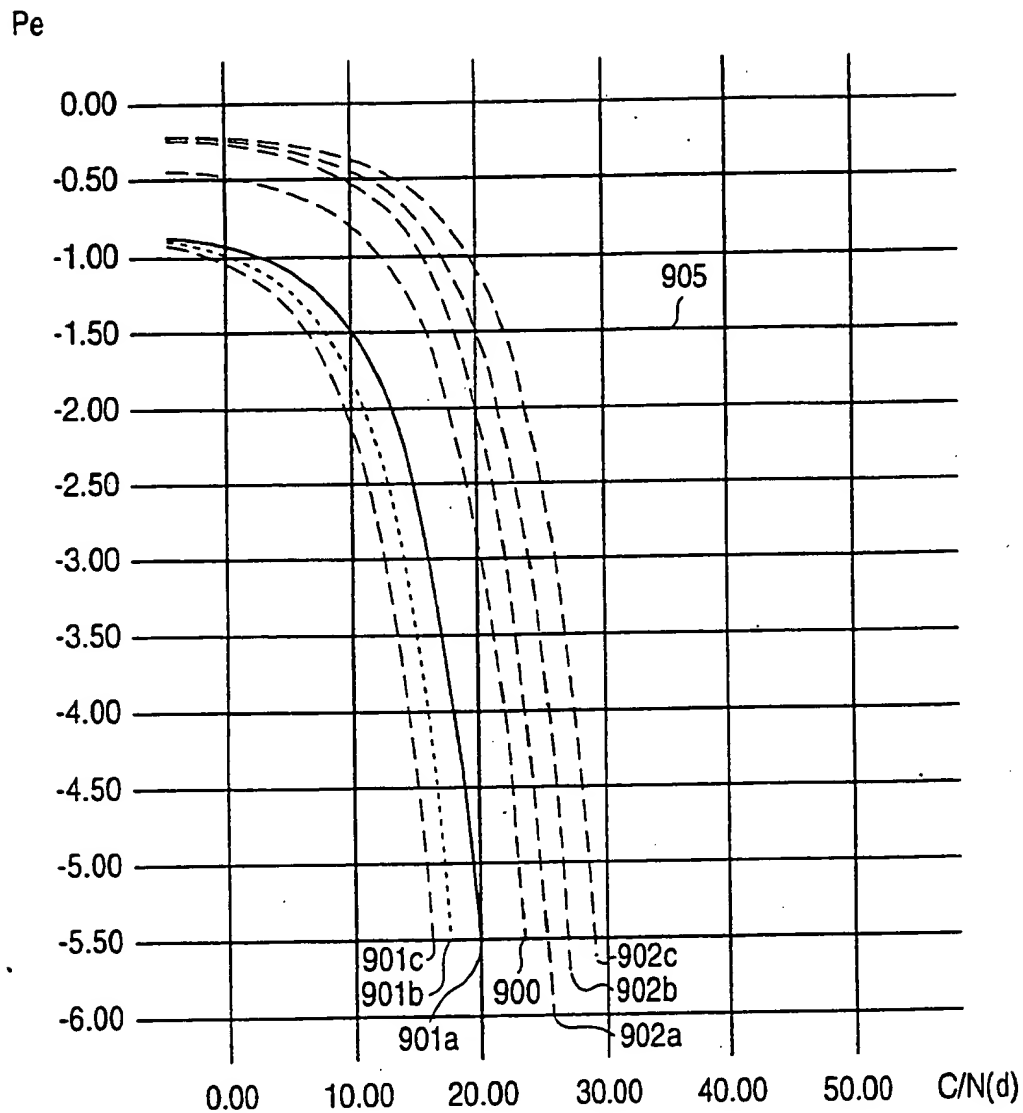


FIG. 102

Pe

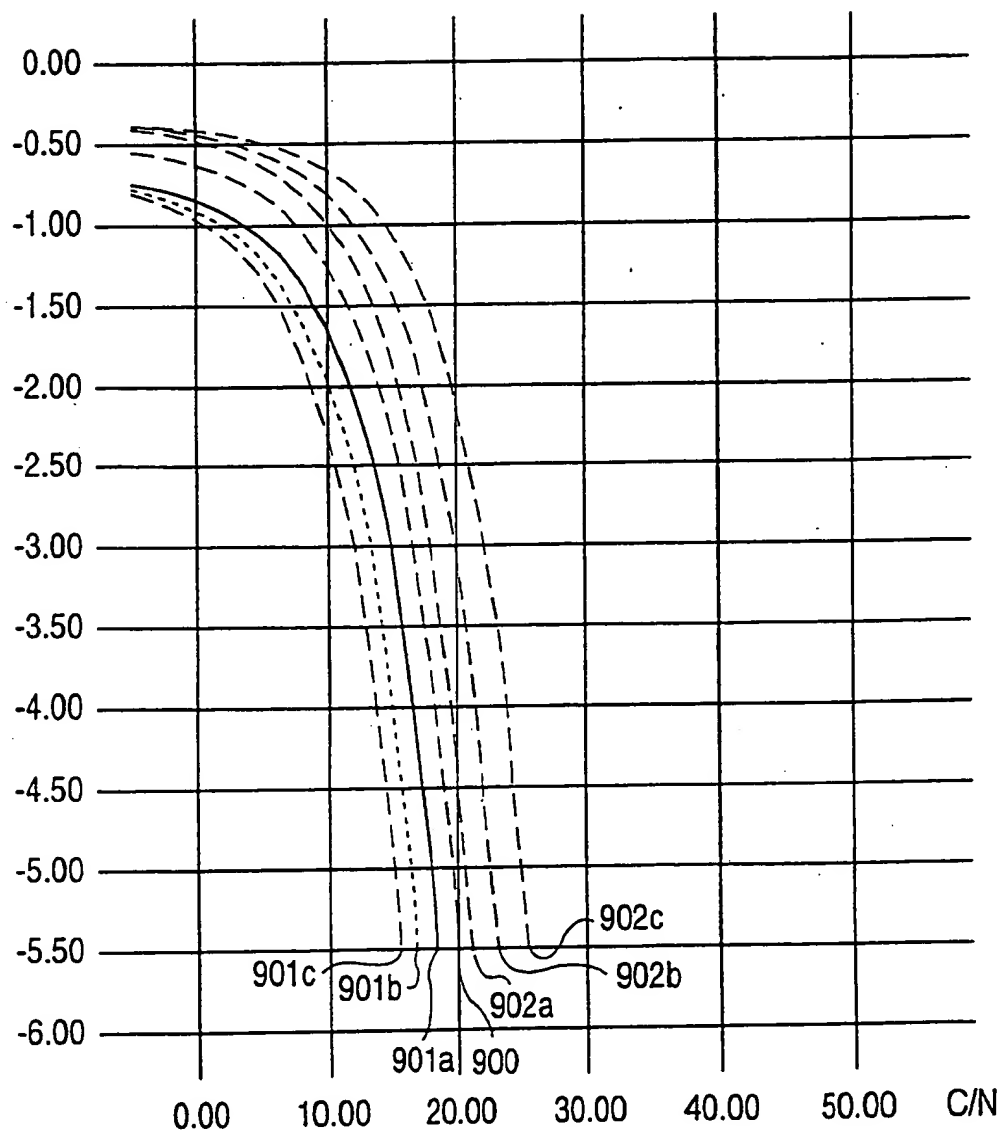


FIG. 103

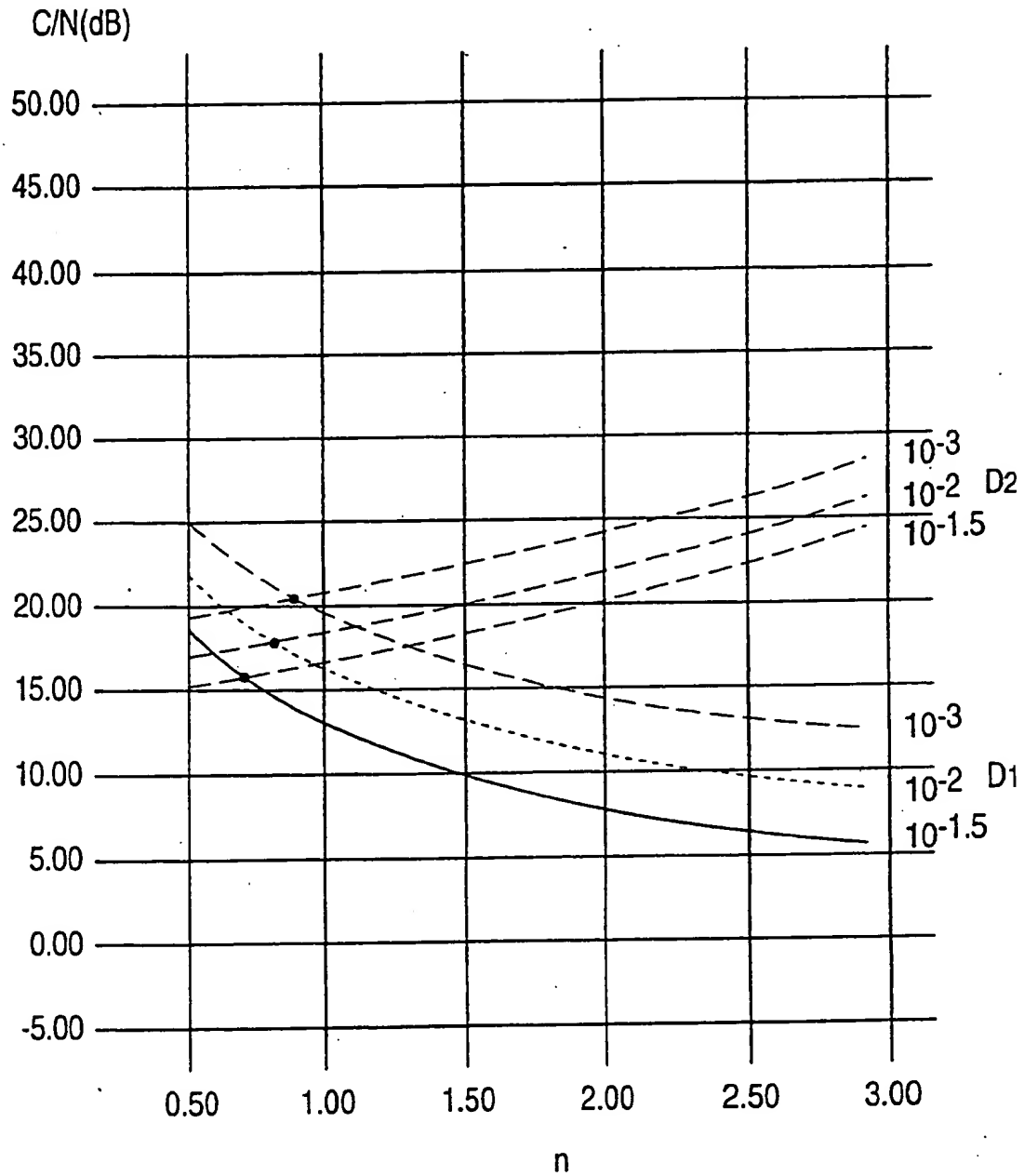


FIG. 104

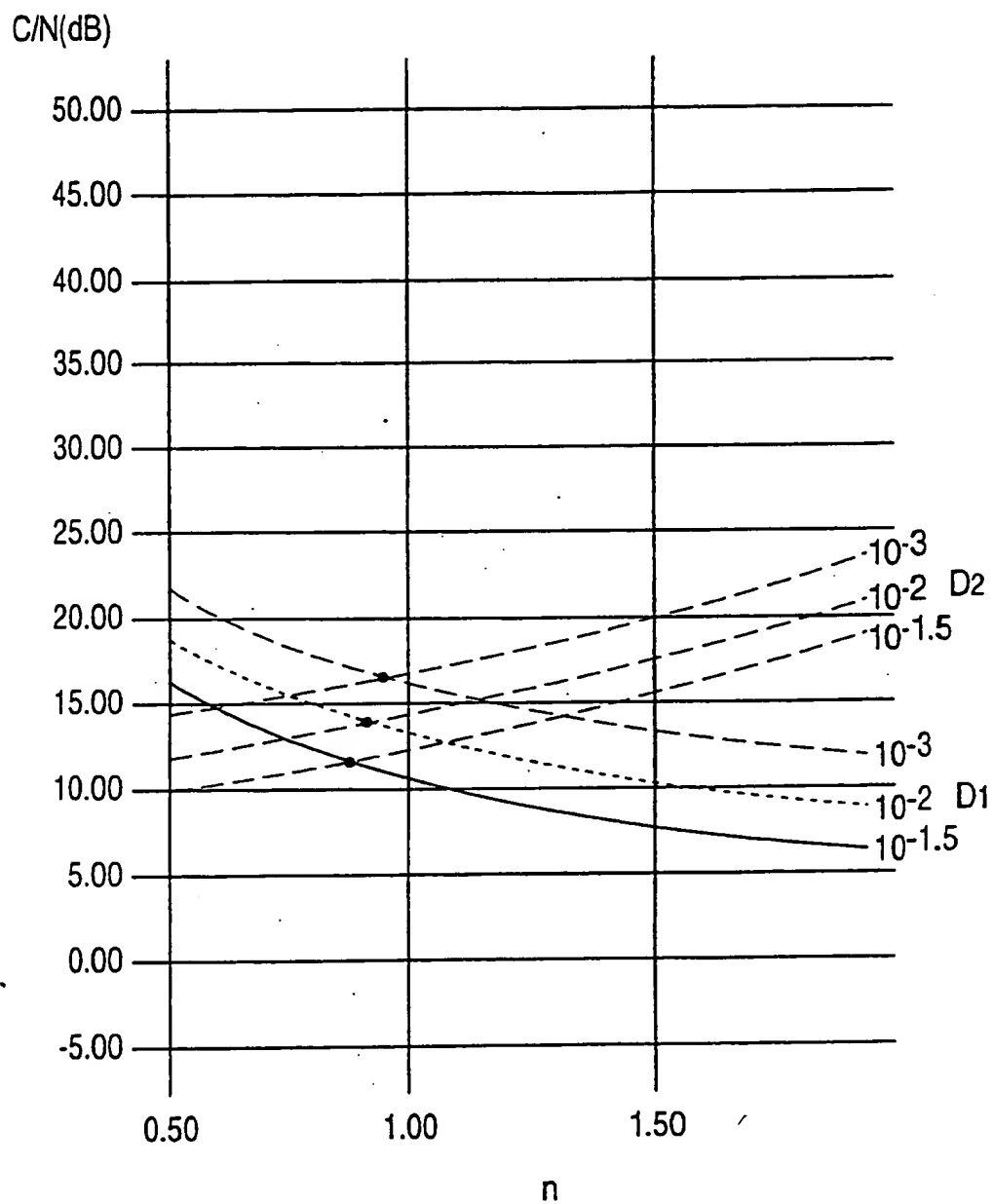


FIG. 105

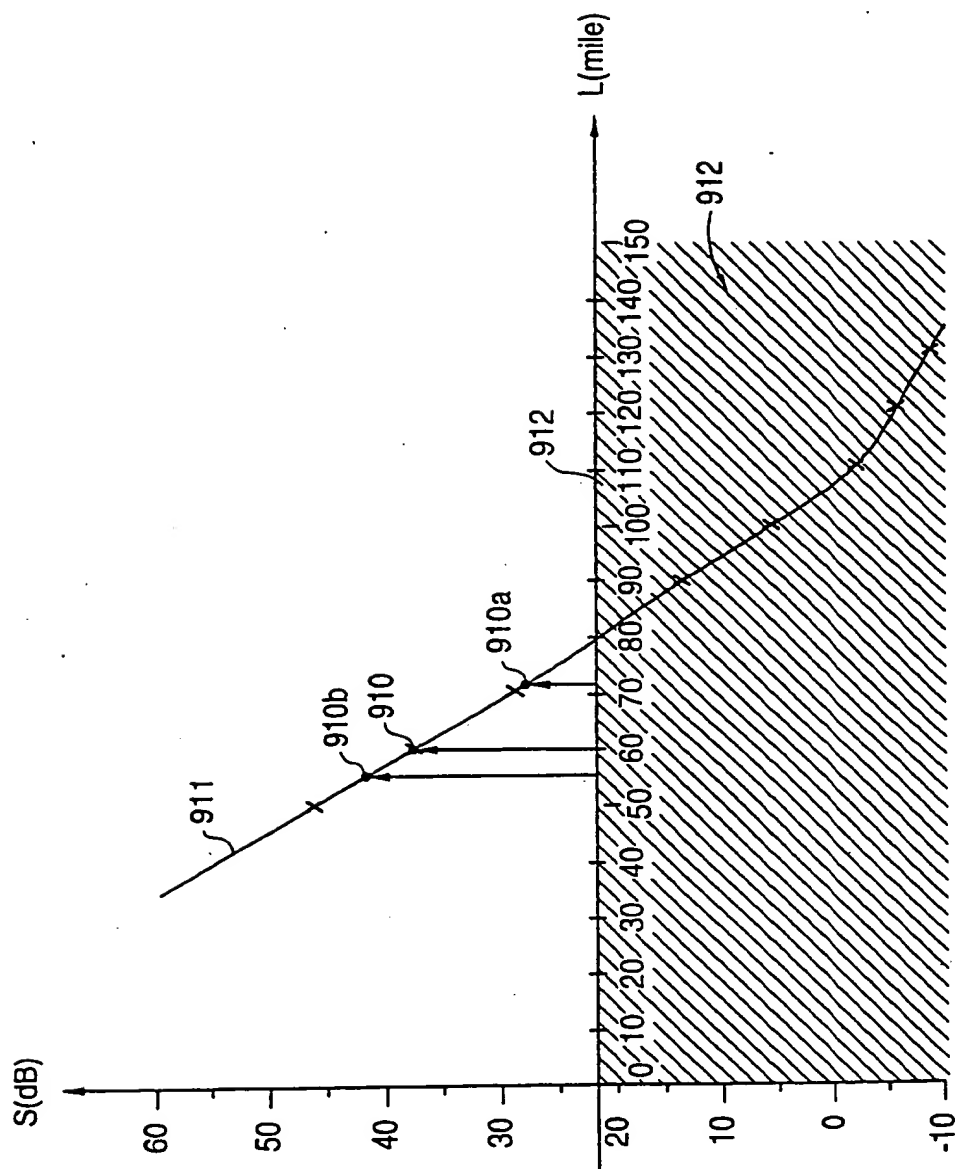


FIG. 106

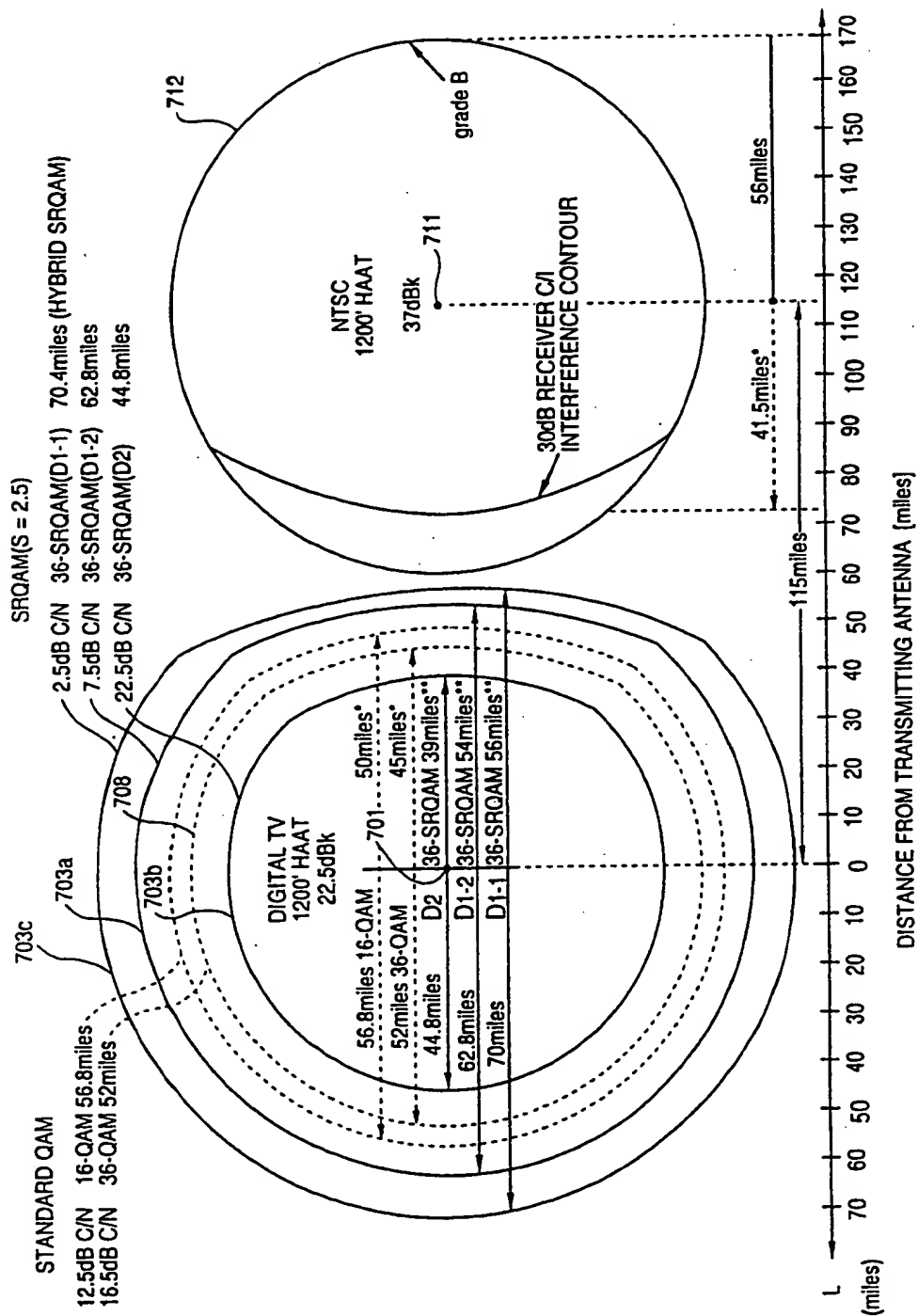


FIG. 107

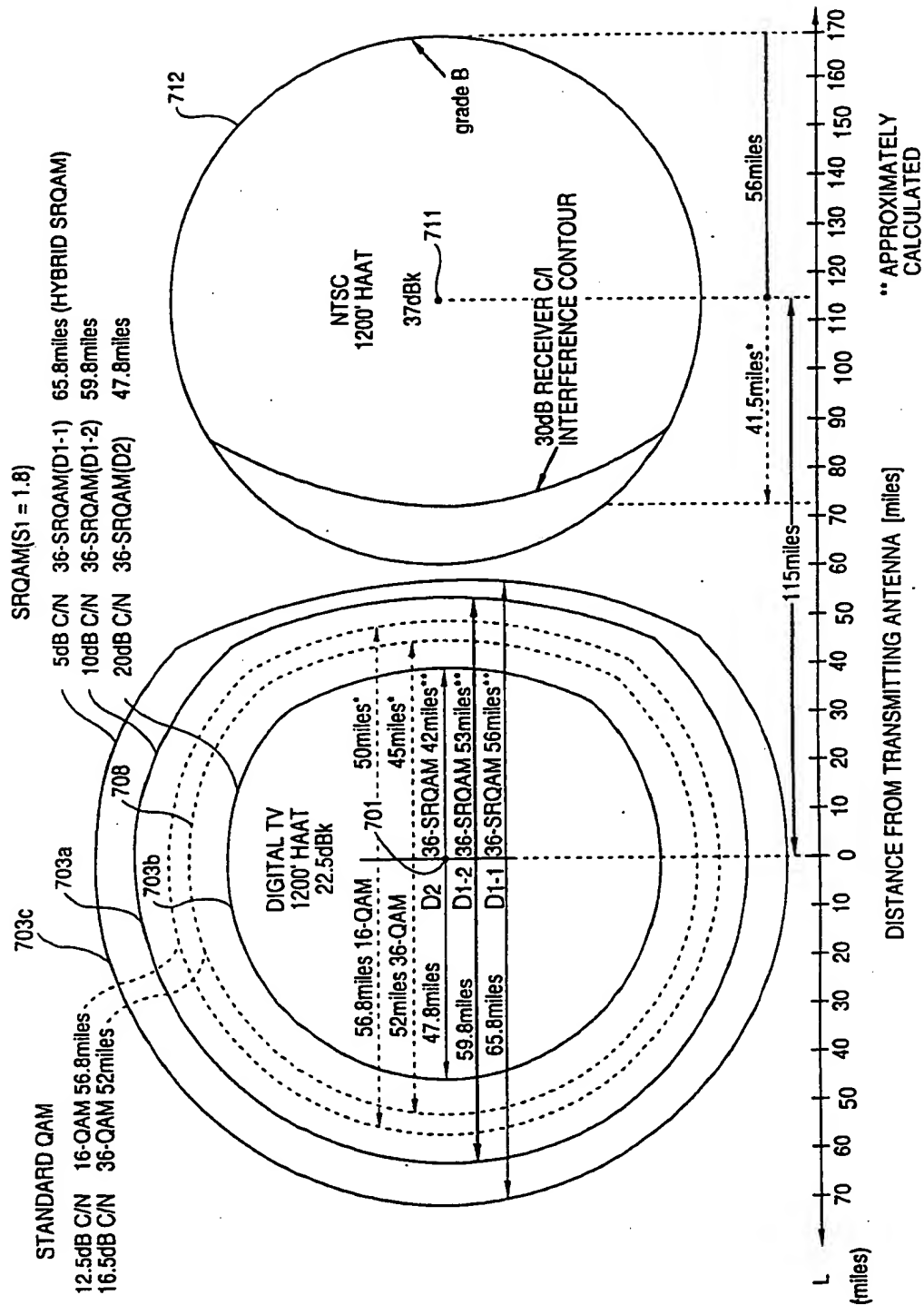


FIG. 108(a)

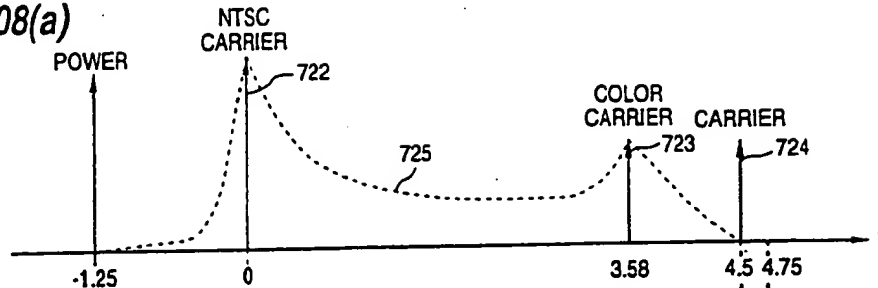


FIG. 108(b)

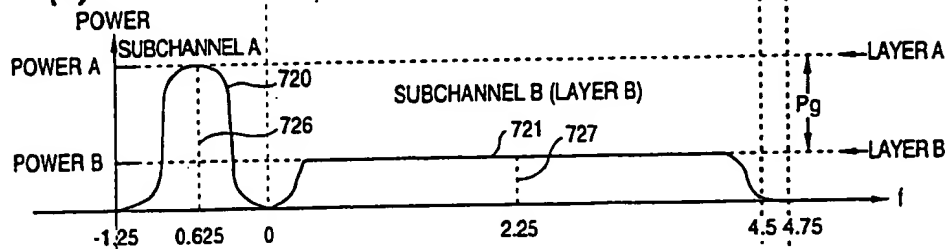


FIG. 108(c)

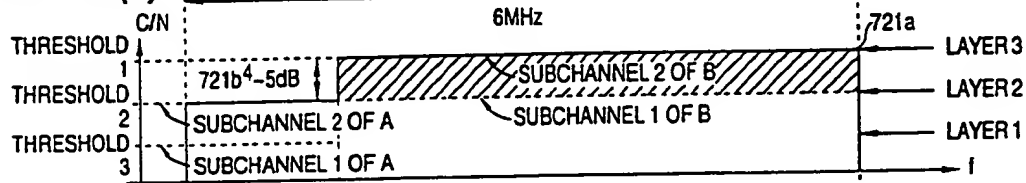


FIG. 108(d)

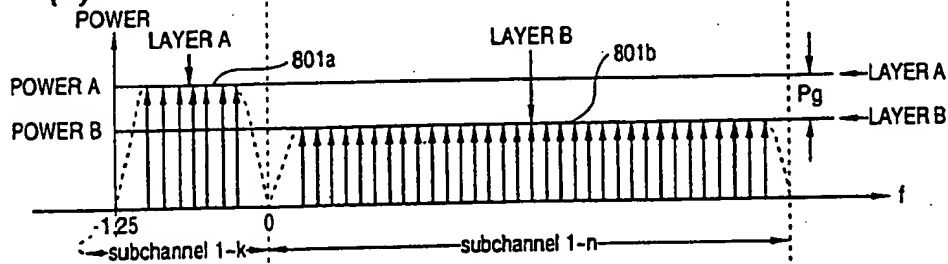


FIG. 108(e)

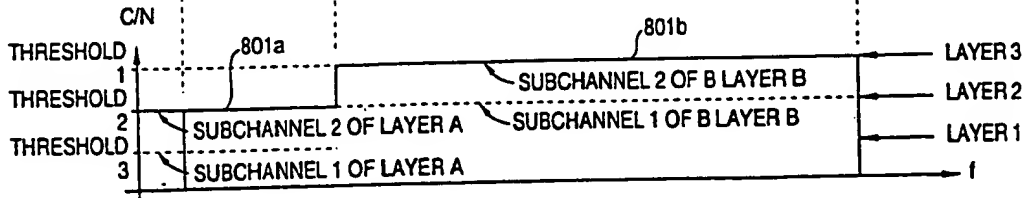


FIG. 109

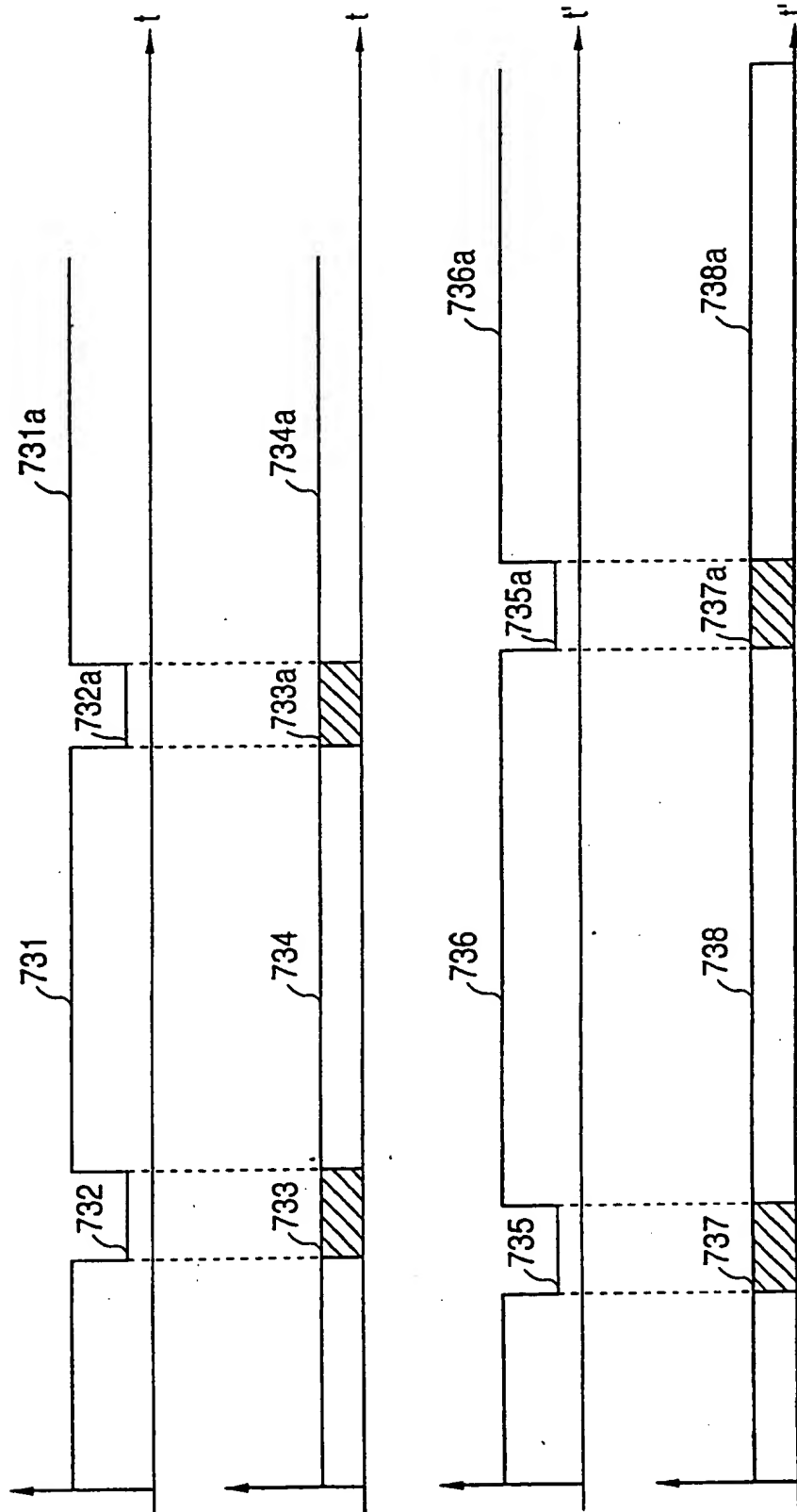


FIG. 110

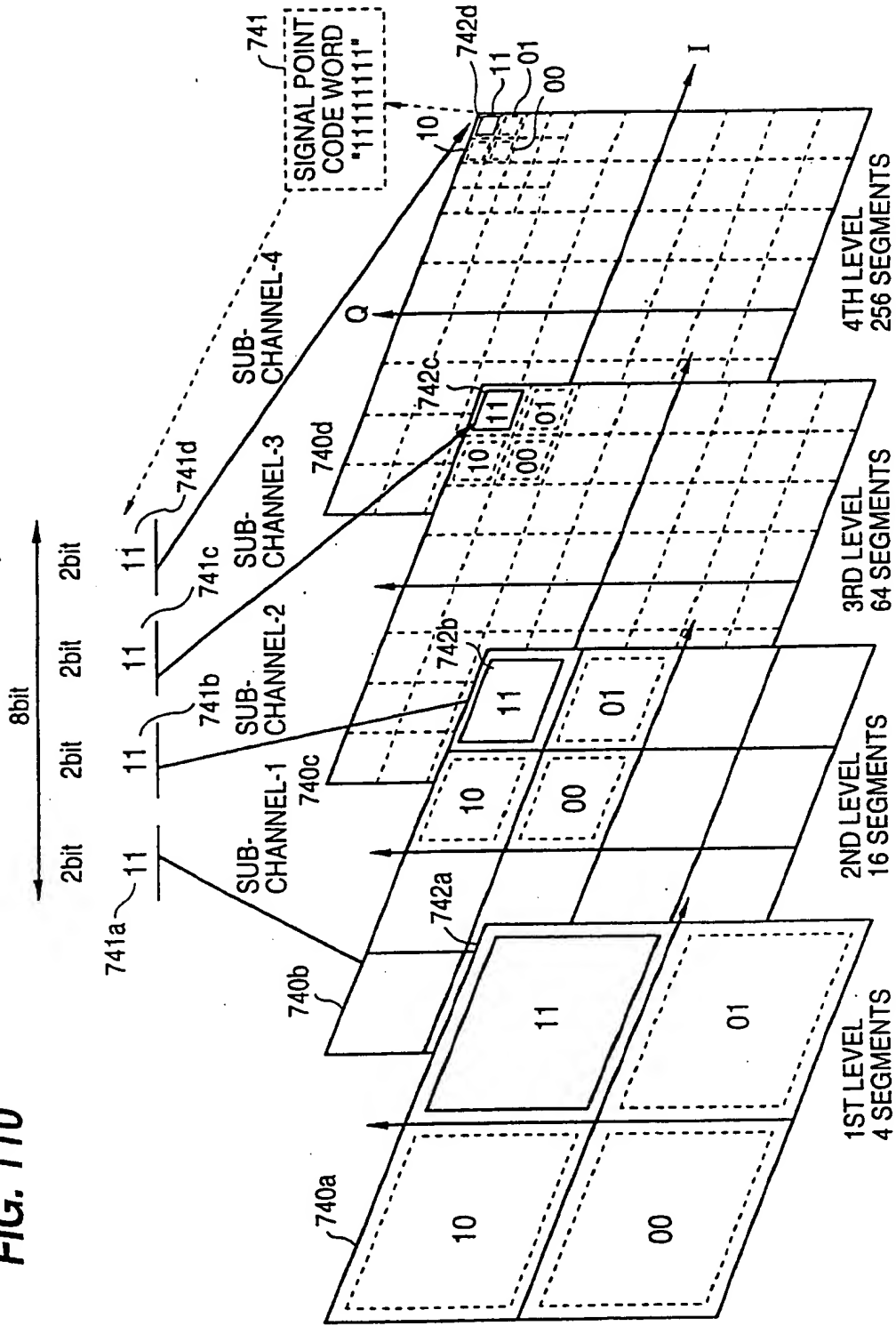
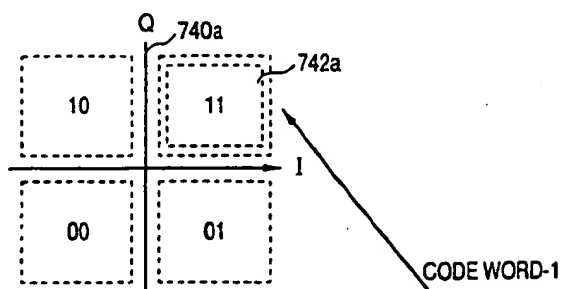
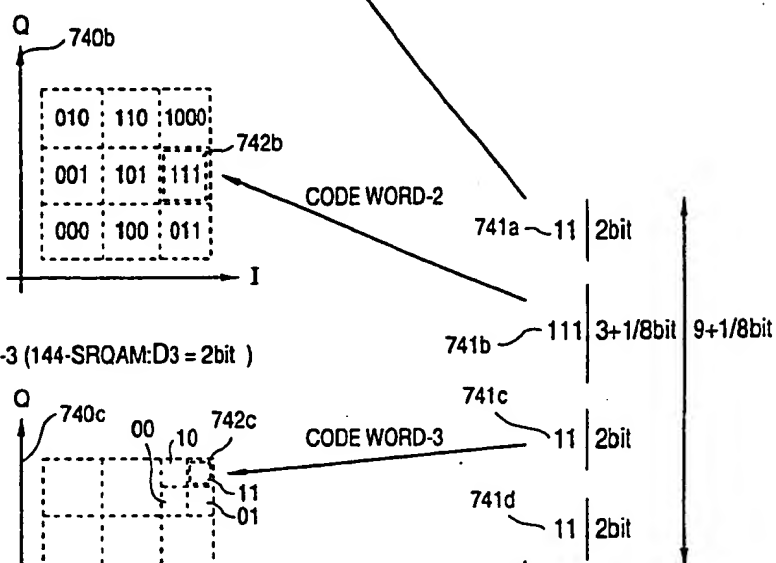


FIG. 111

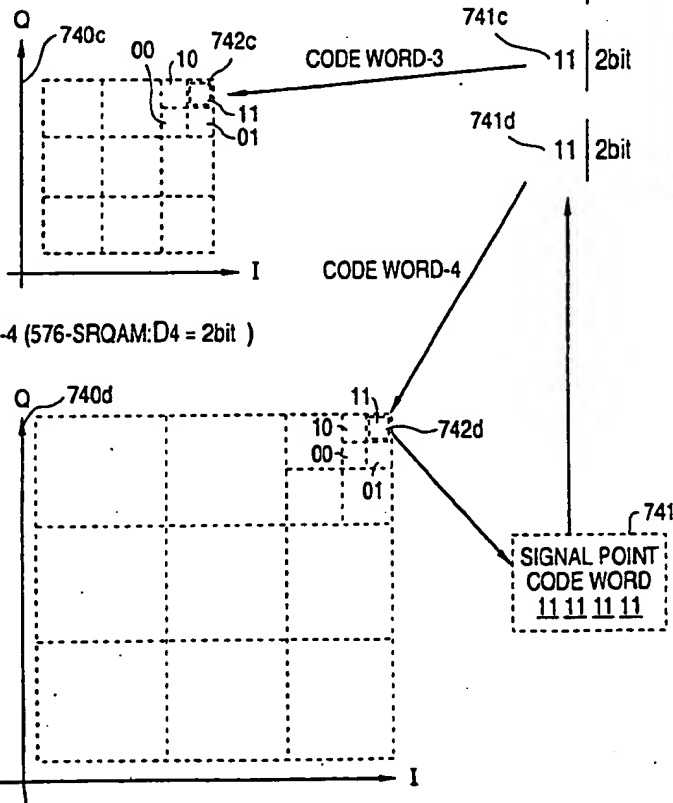
SUBCHANNEL-1 (SRQAM:D1 = 2bit)



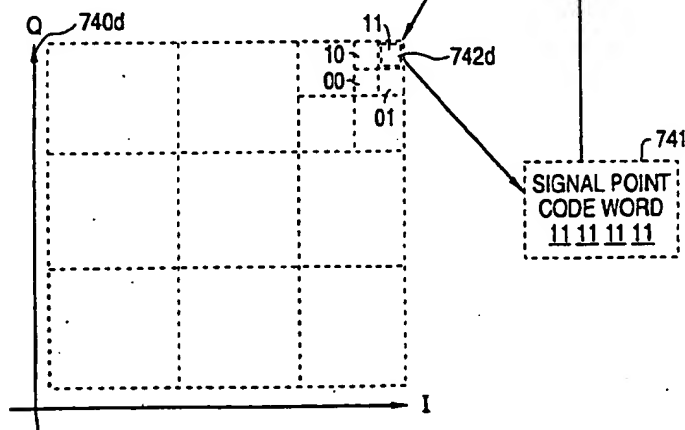
SUBCHANNEL-2 (36-SRQAM:D2 = 3bit + 1/8bit)



SUBCHANNEL-3 (144-SRQAM:D3 = 2bit)



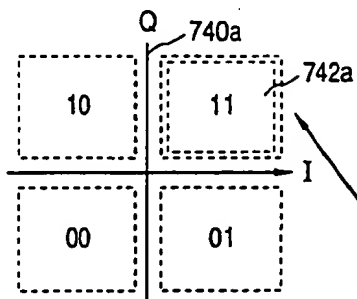
SUBCHANNEL-4 (576-SRQAM:D4 = 2bit)



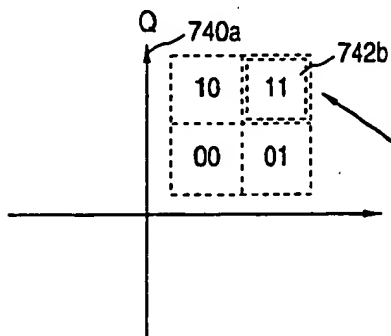
SIGNAL POINT  
CODE WORD  
11 11 11 11

FIG. 112

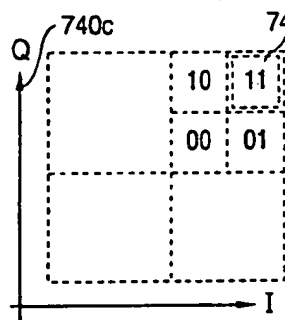
SUBCHANNEL-1 (SRQAM:D1 = 2bit)



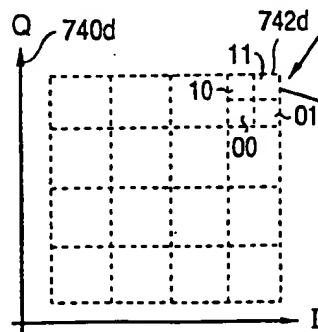
SUBCHANNEL-2 (16-SRQAM:D2 = 2bit)



SUBCHANNEL-3 (64-SRQAM:D3 = 2bit)



SUBCHANNEL-4 (256-SRQAM:D4 = 2bit)

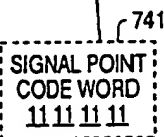
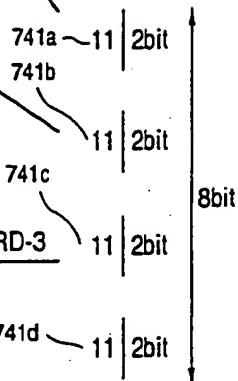


CODE WORD-1

CODE WORD-2

CODE WORD-3

CODE WORD-4



00000110000

**FIG. 113**

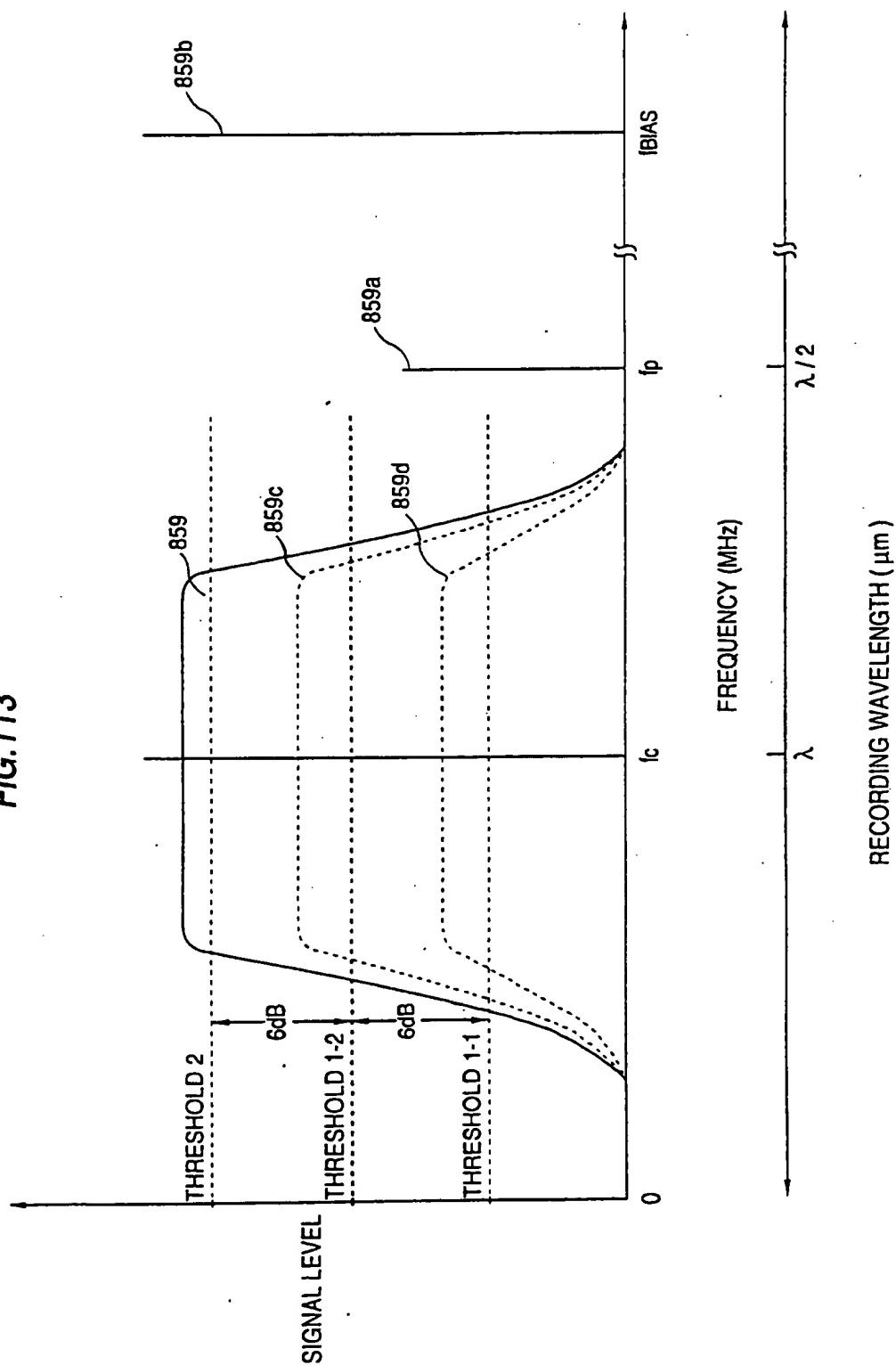


FIG. 114

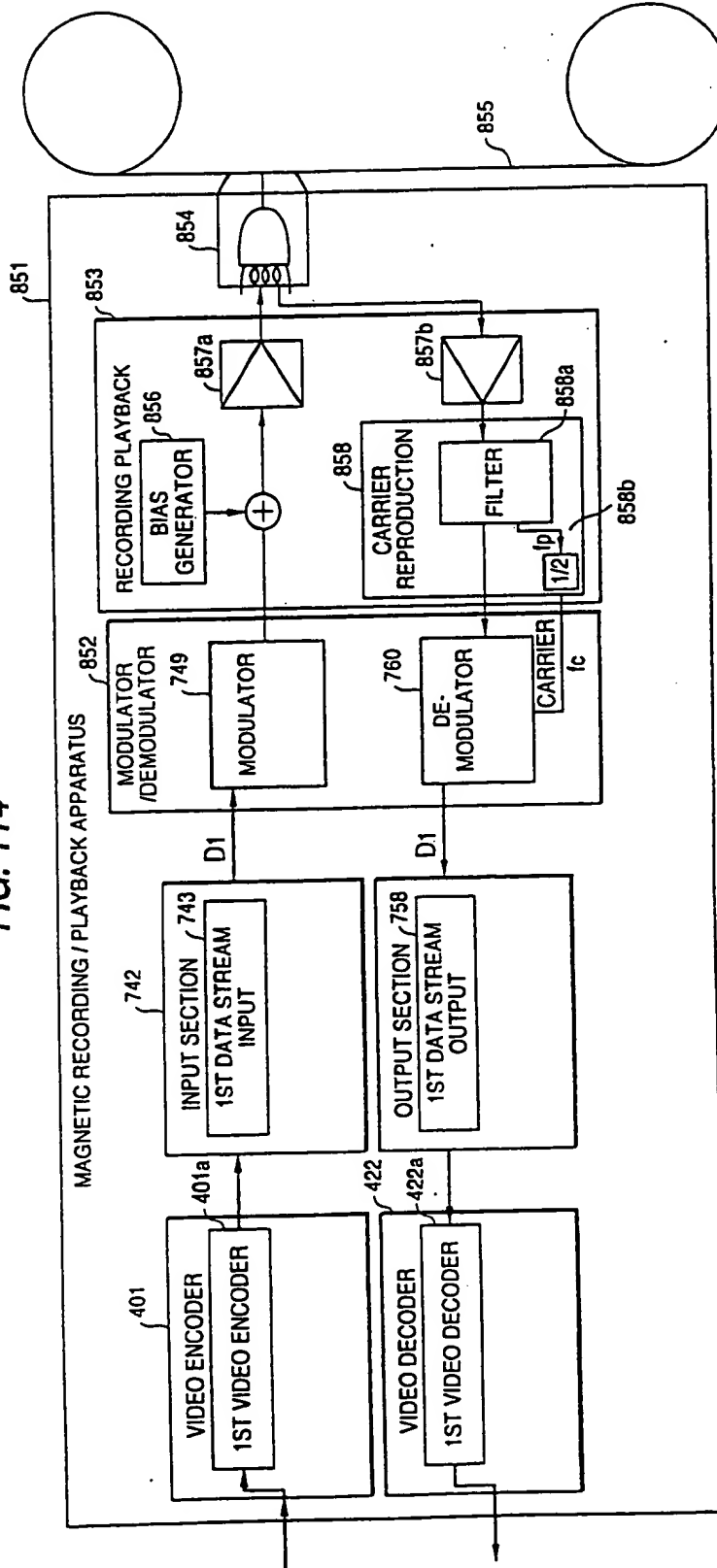


FIG. 115

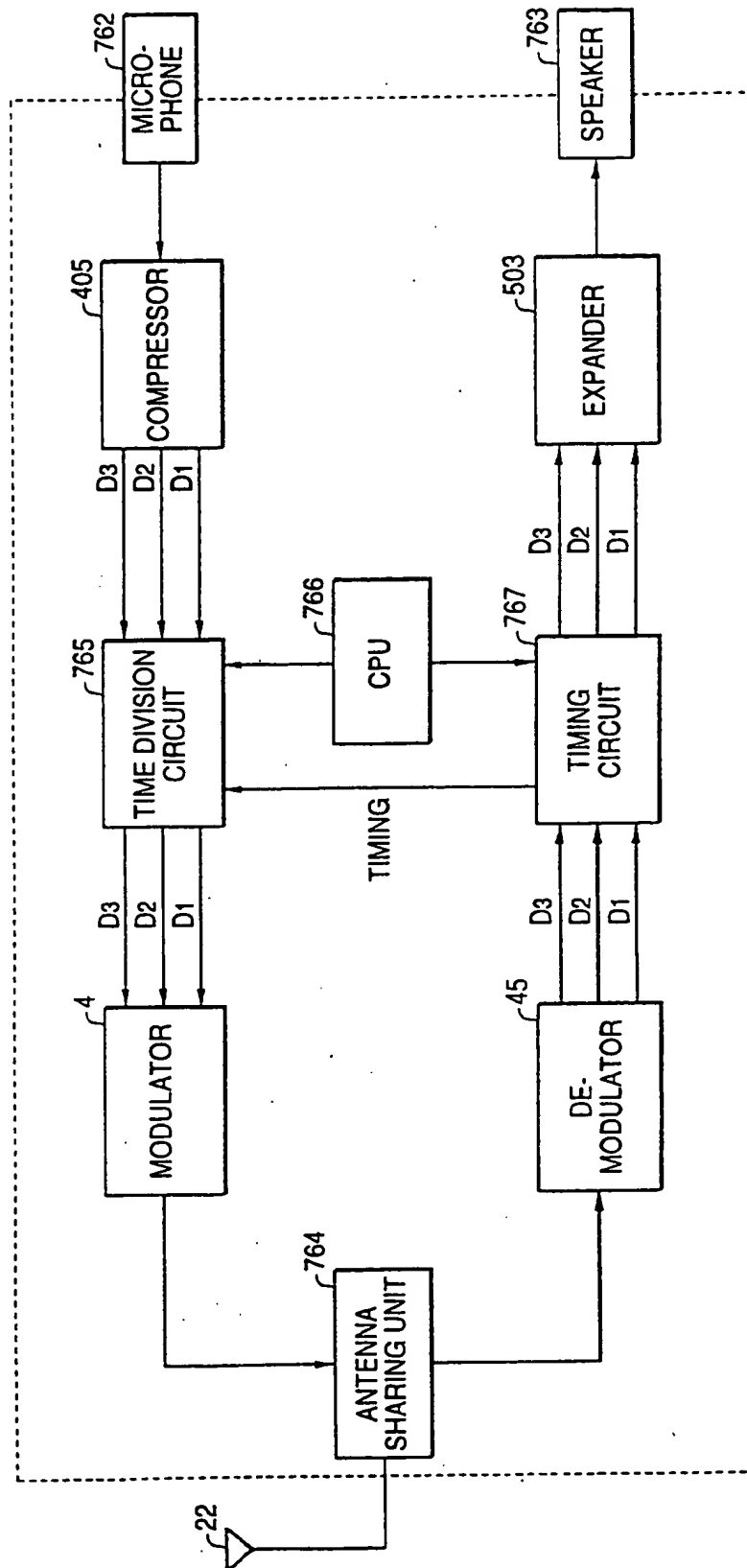


FIG. 116

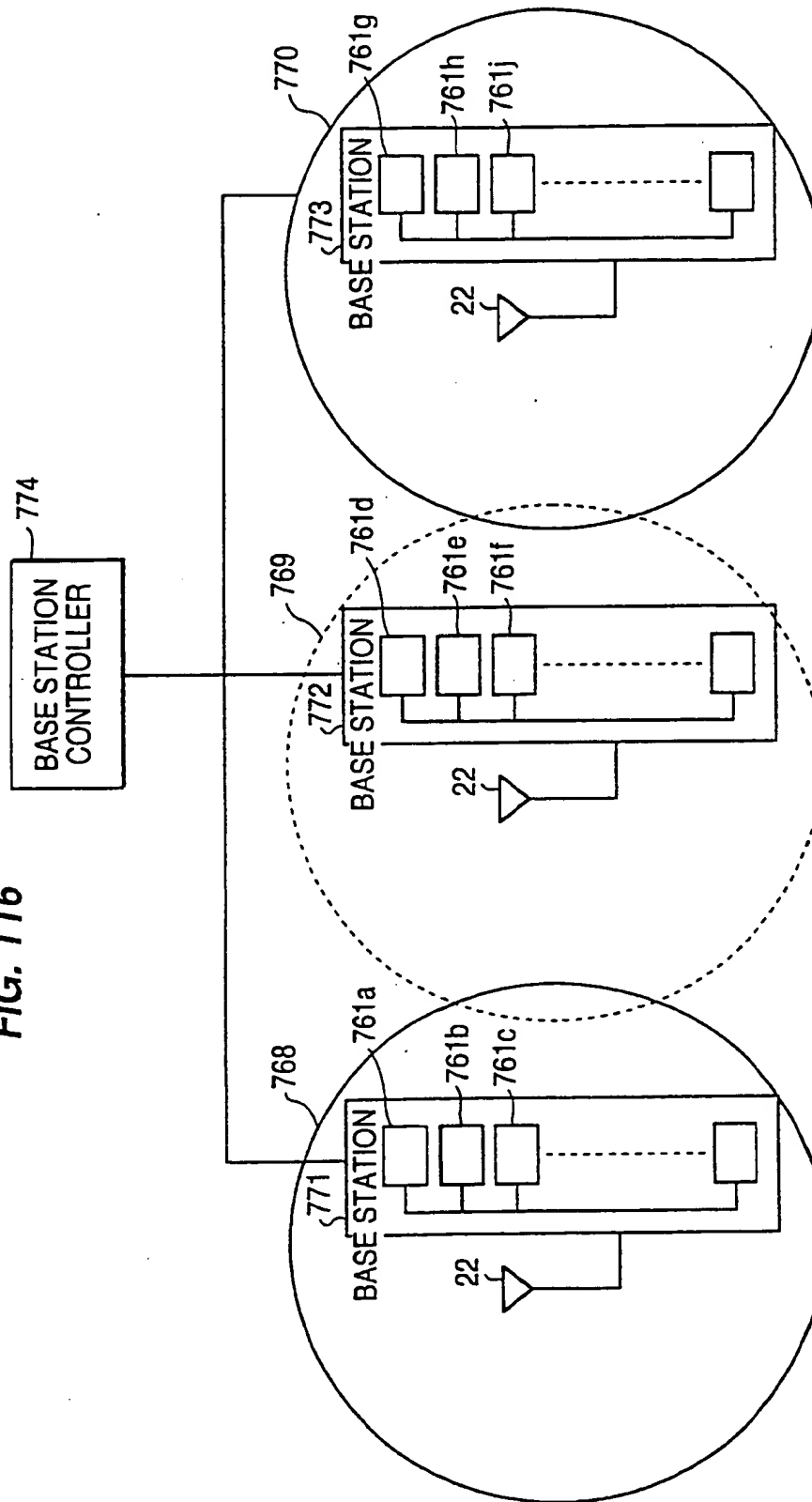
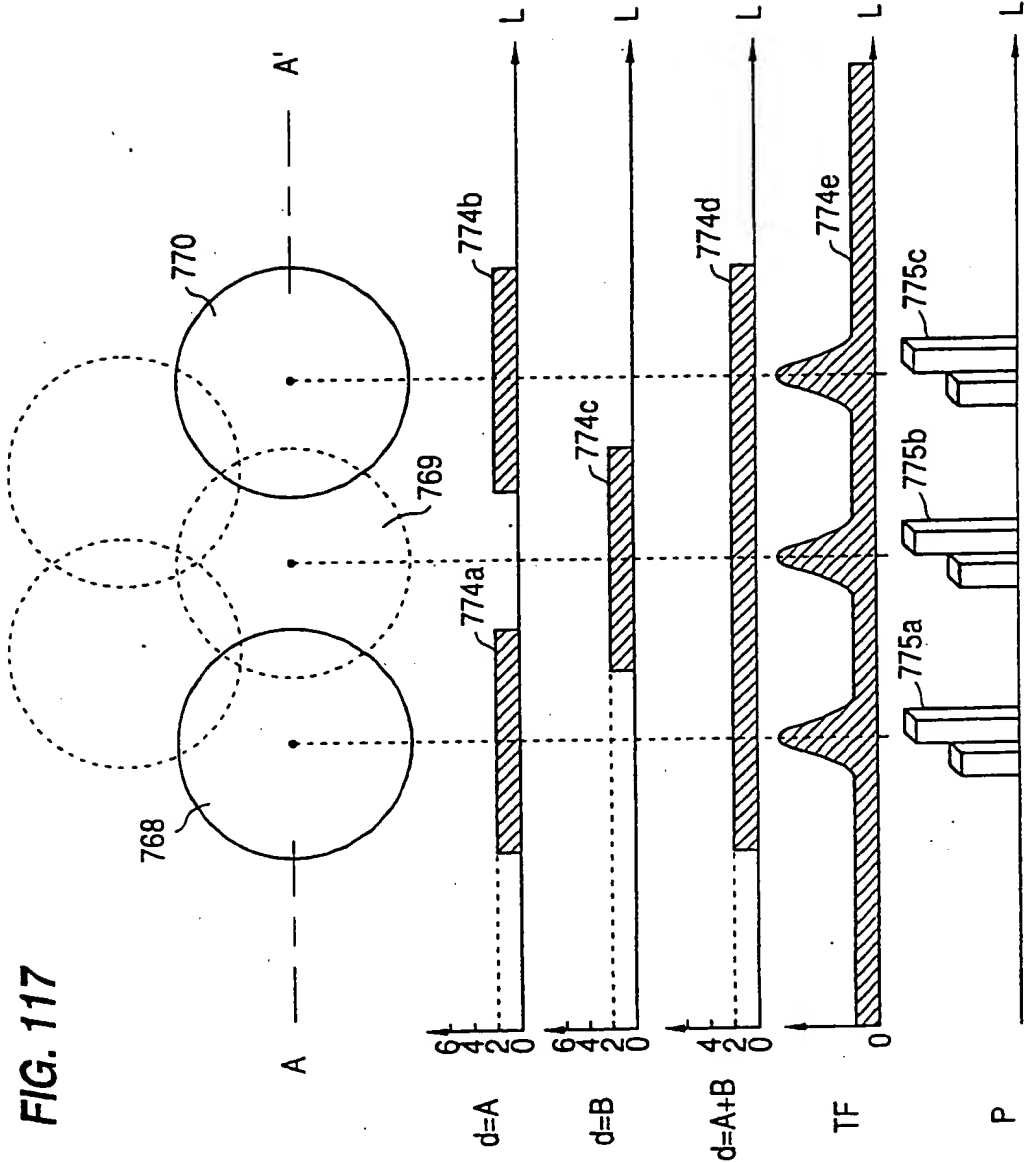


FIG. 117



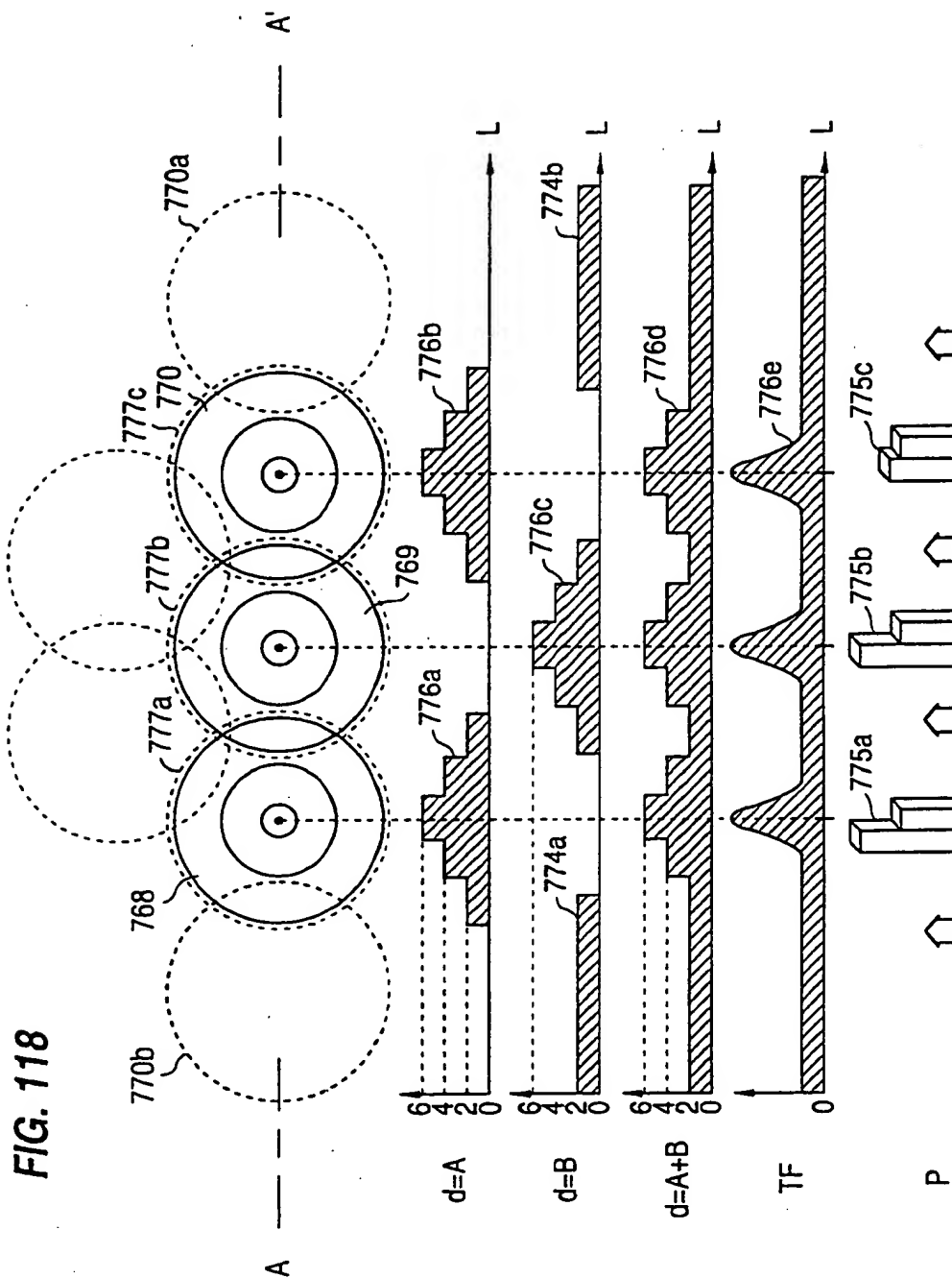


FIG. 119(a)

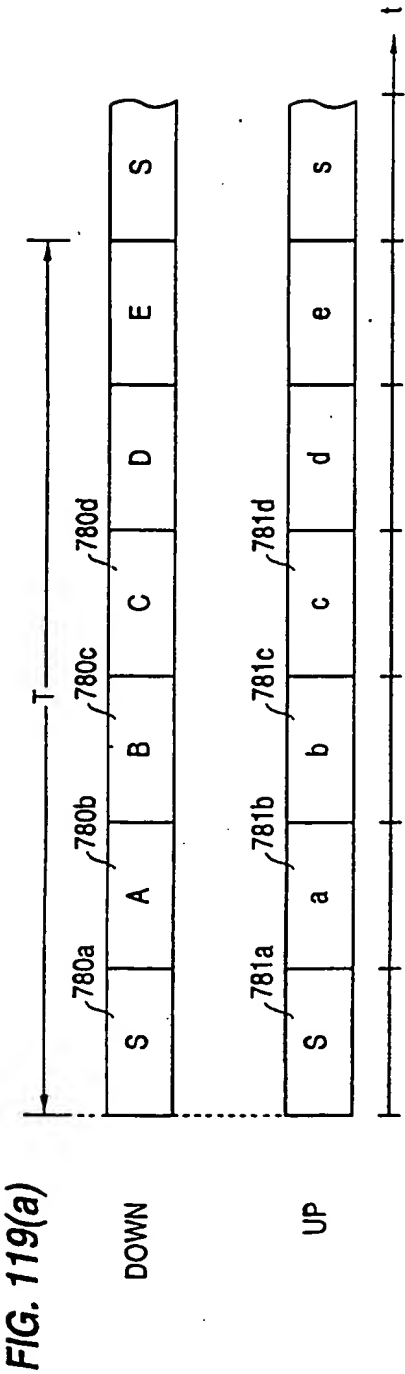


FIG. 119(b)

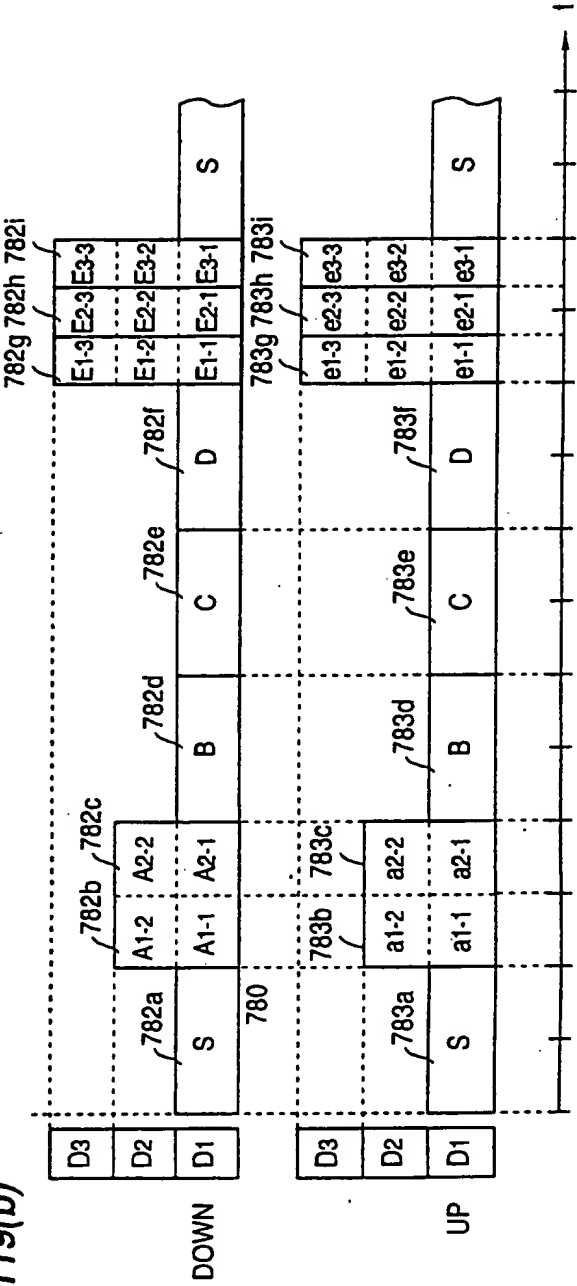




FIG. 121

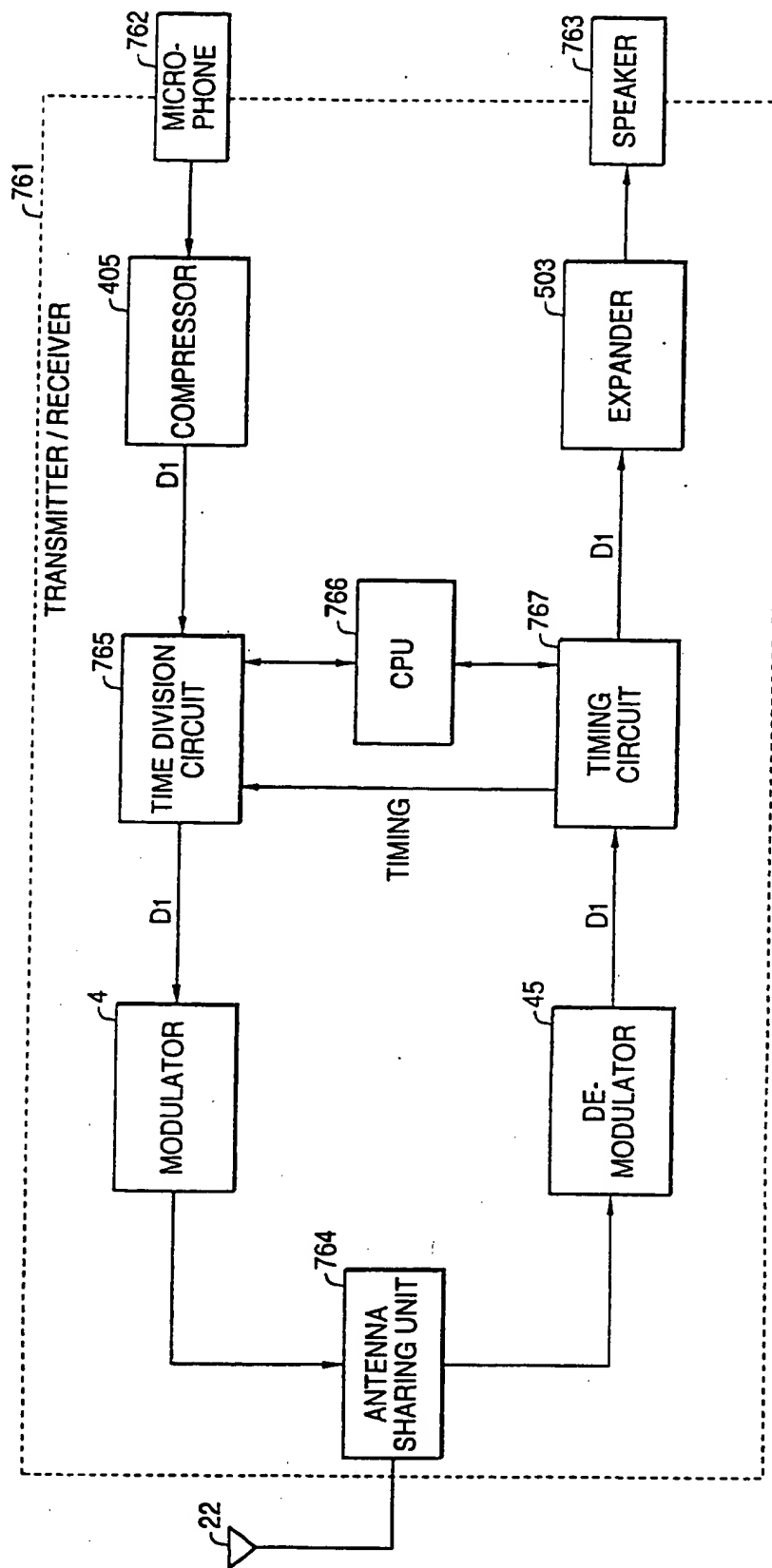
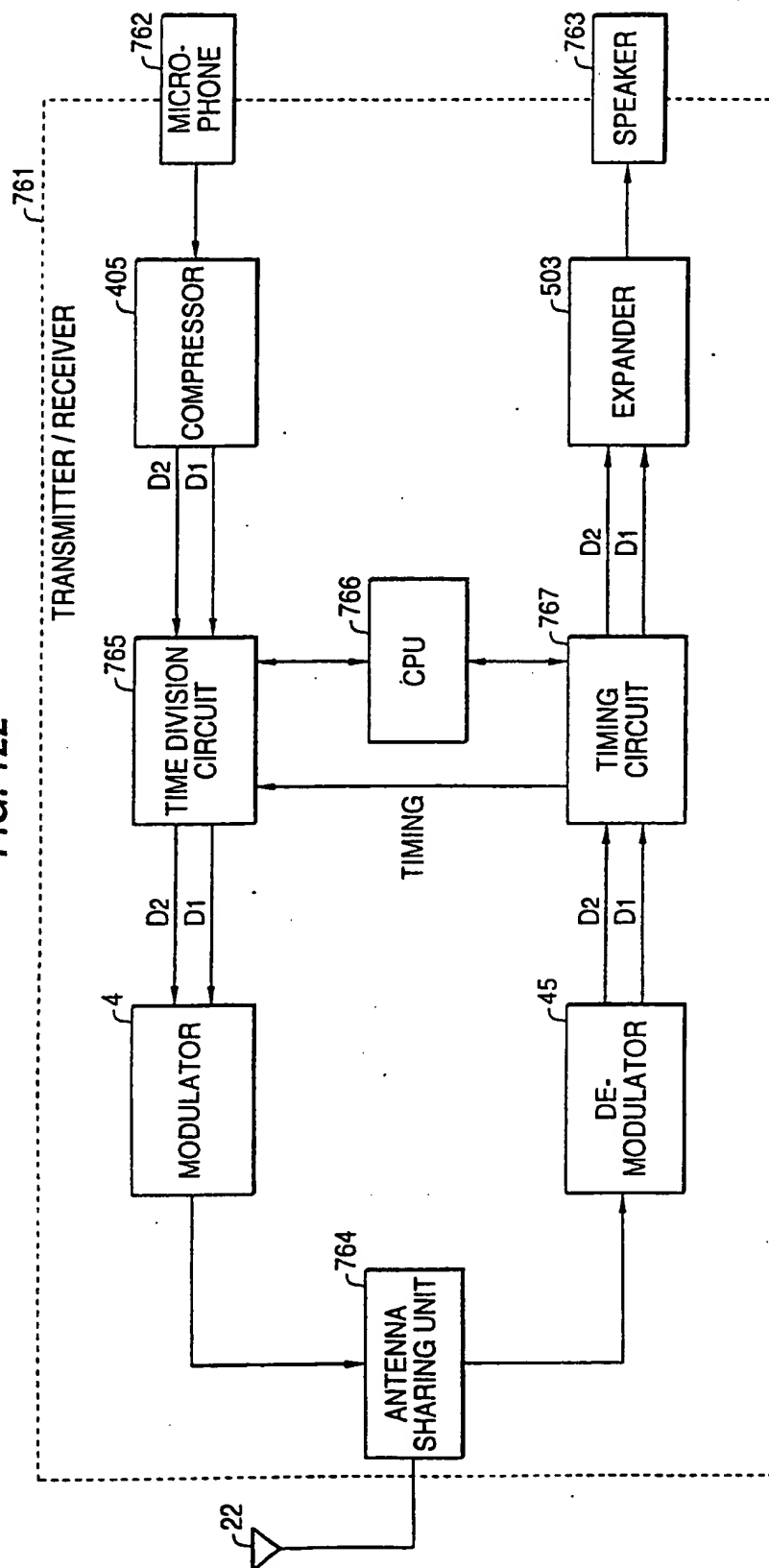
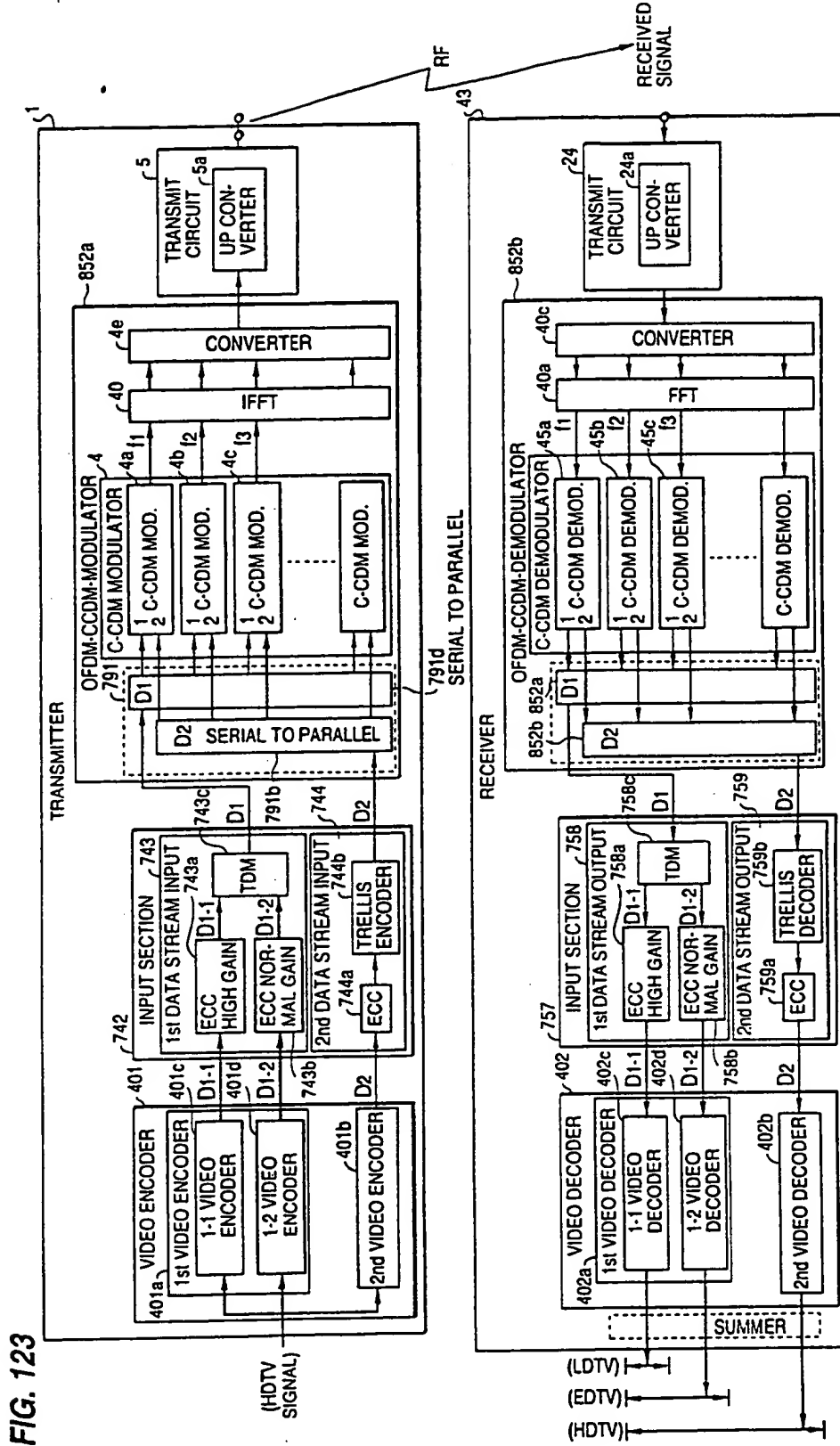


FIG. 122





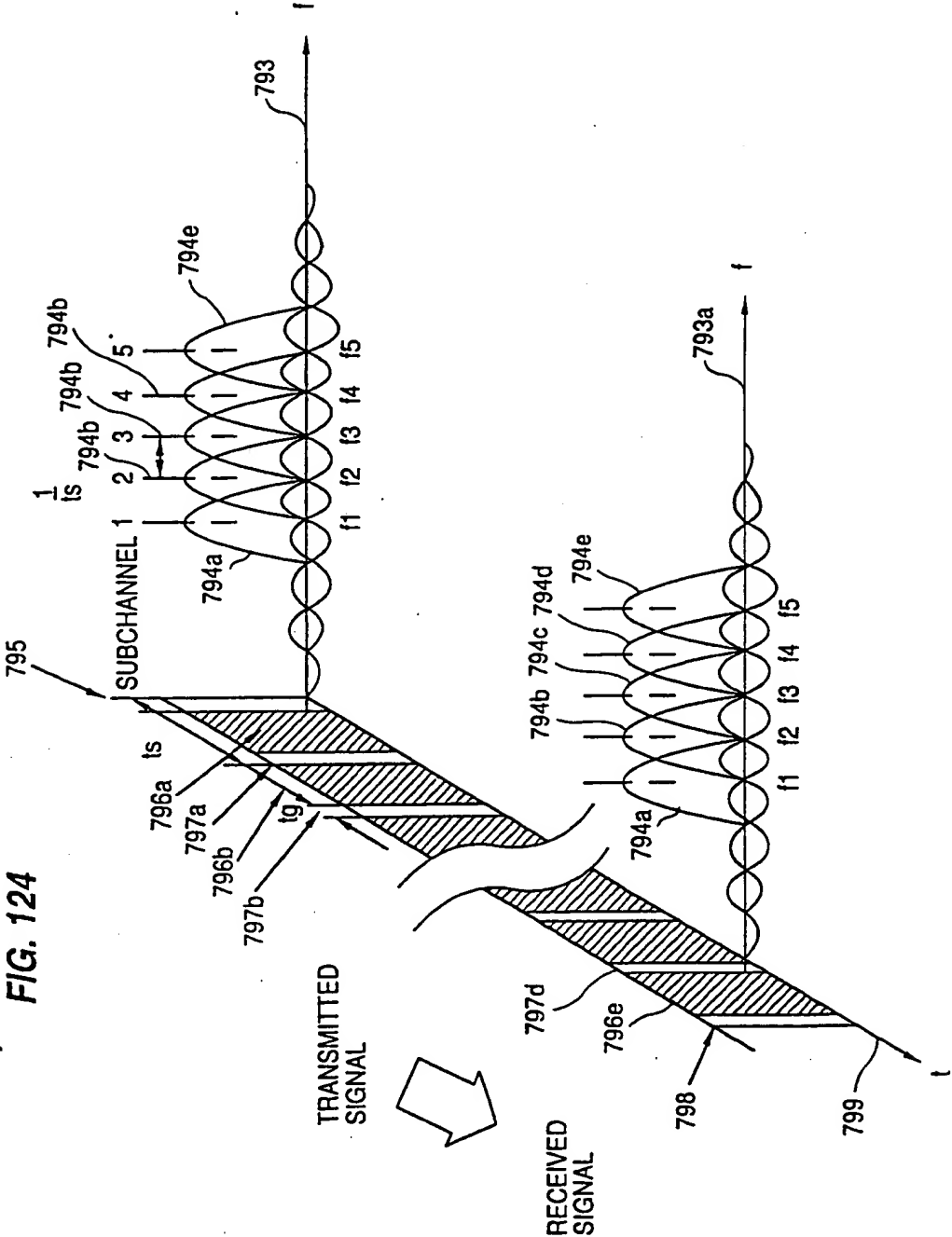


FIG. 125(a)

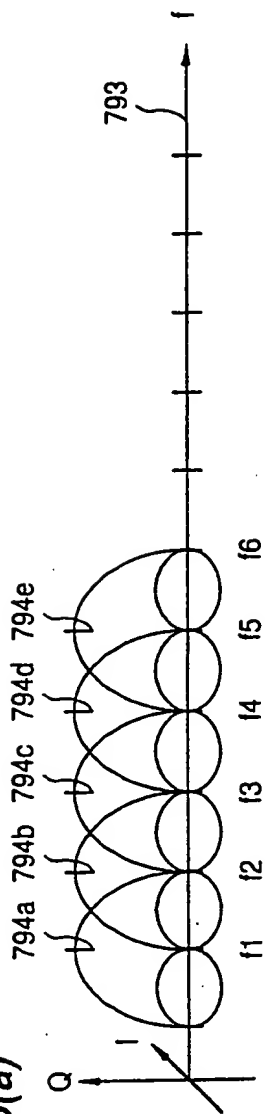
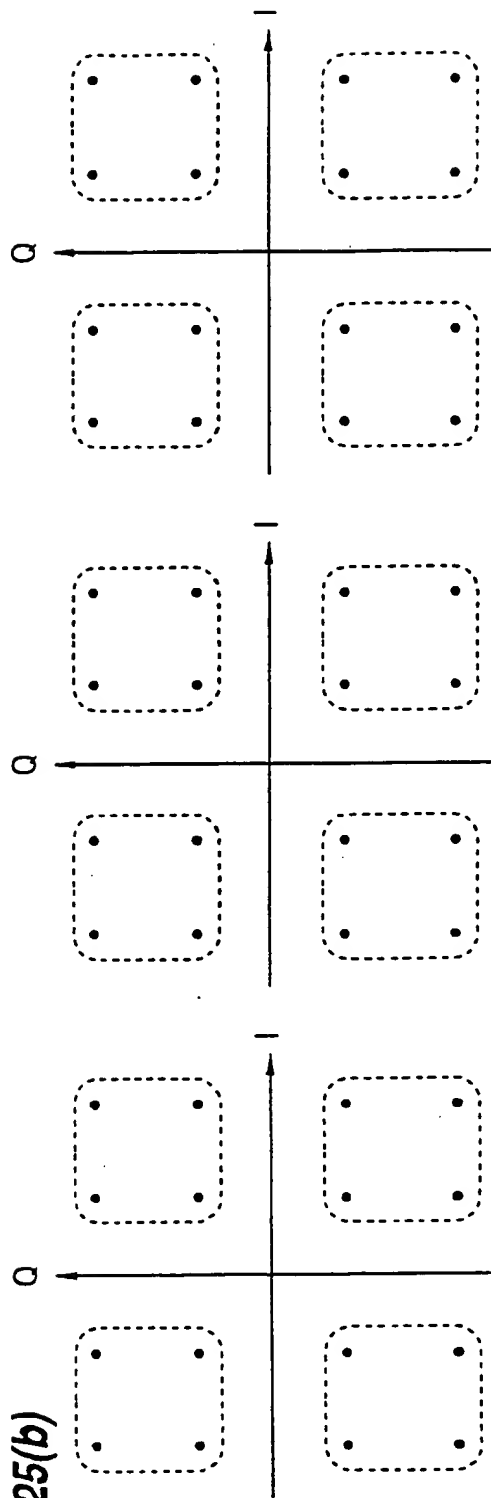


FIG. 125(b)



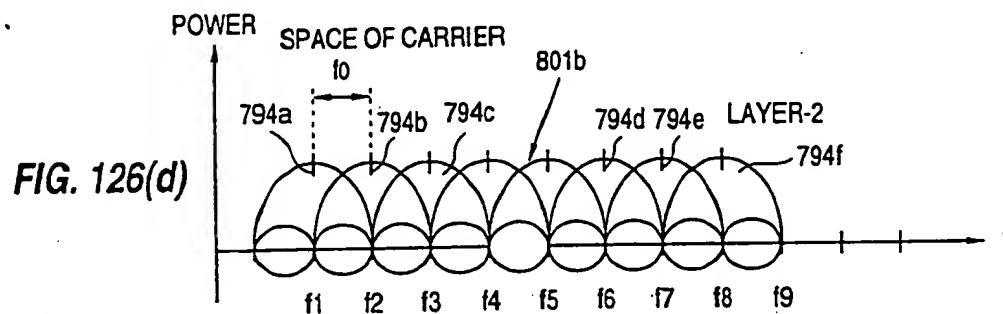
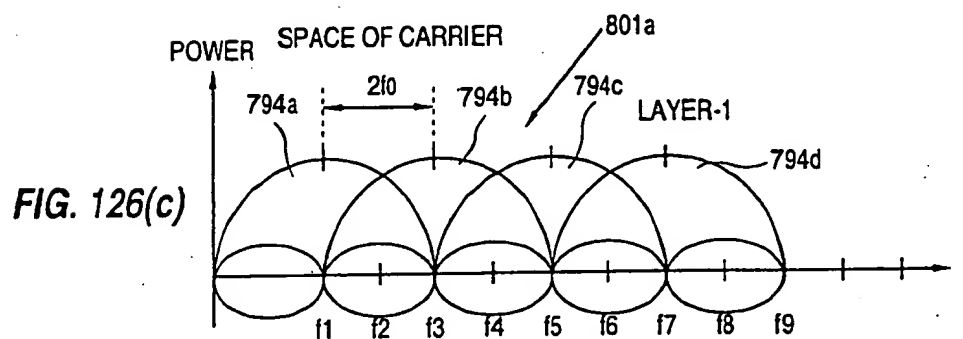
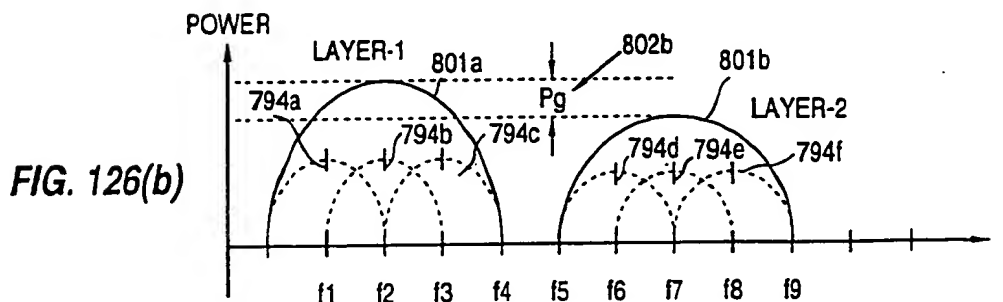
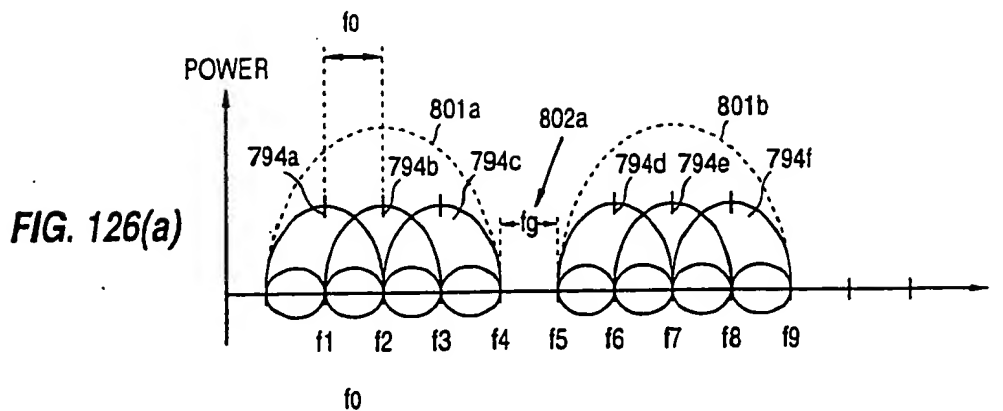


FIG. 127

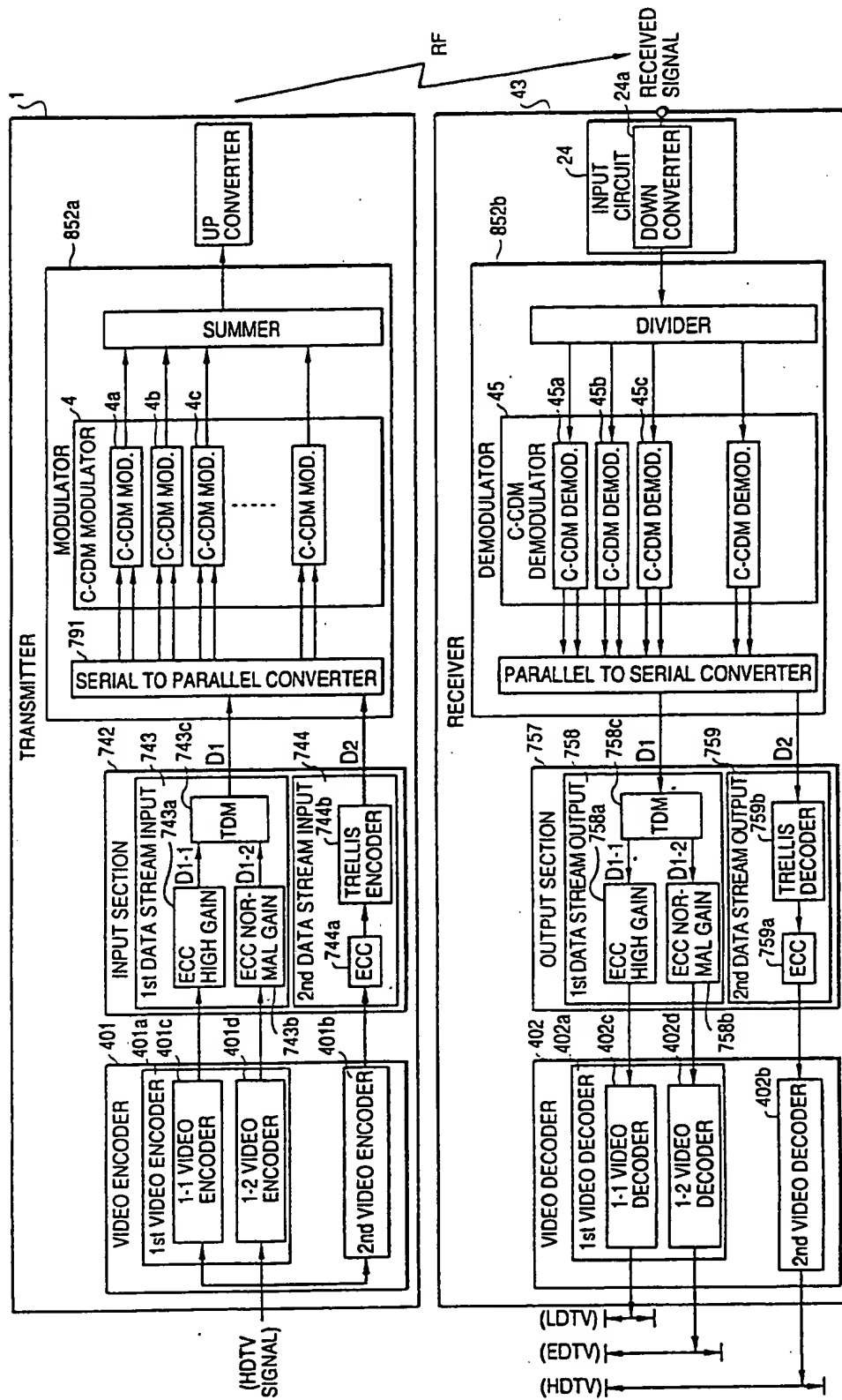


FIG. 128(a)

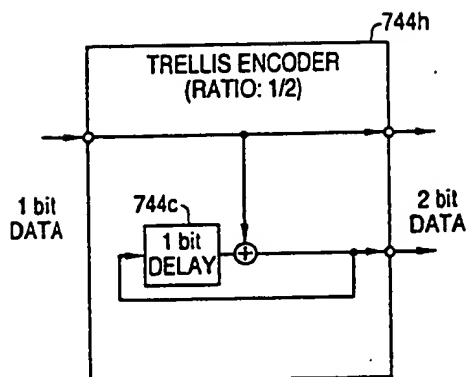


FIG. 128(d)

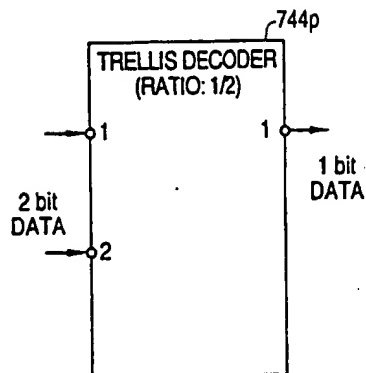


FIG. 128(b)

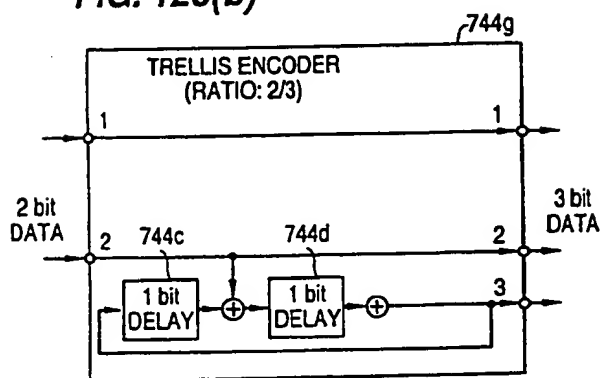


FIG. 128(e)

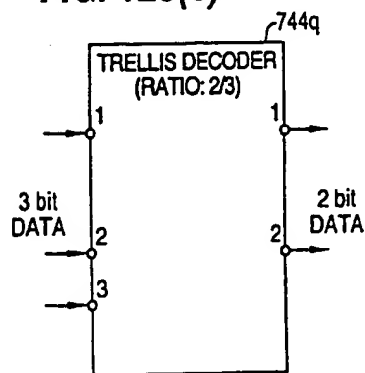


FIG. 128(c)

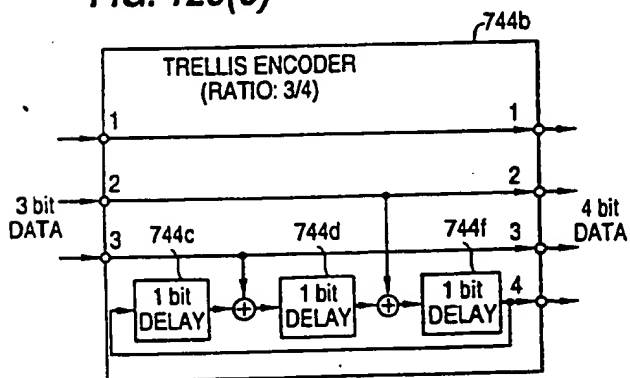


FIG. 128(f)

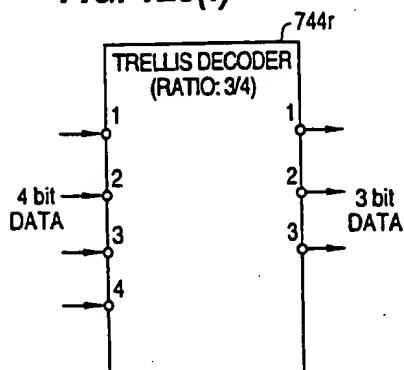


FIG. 129

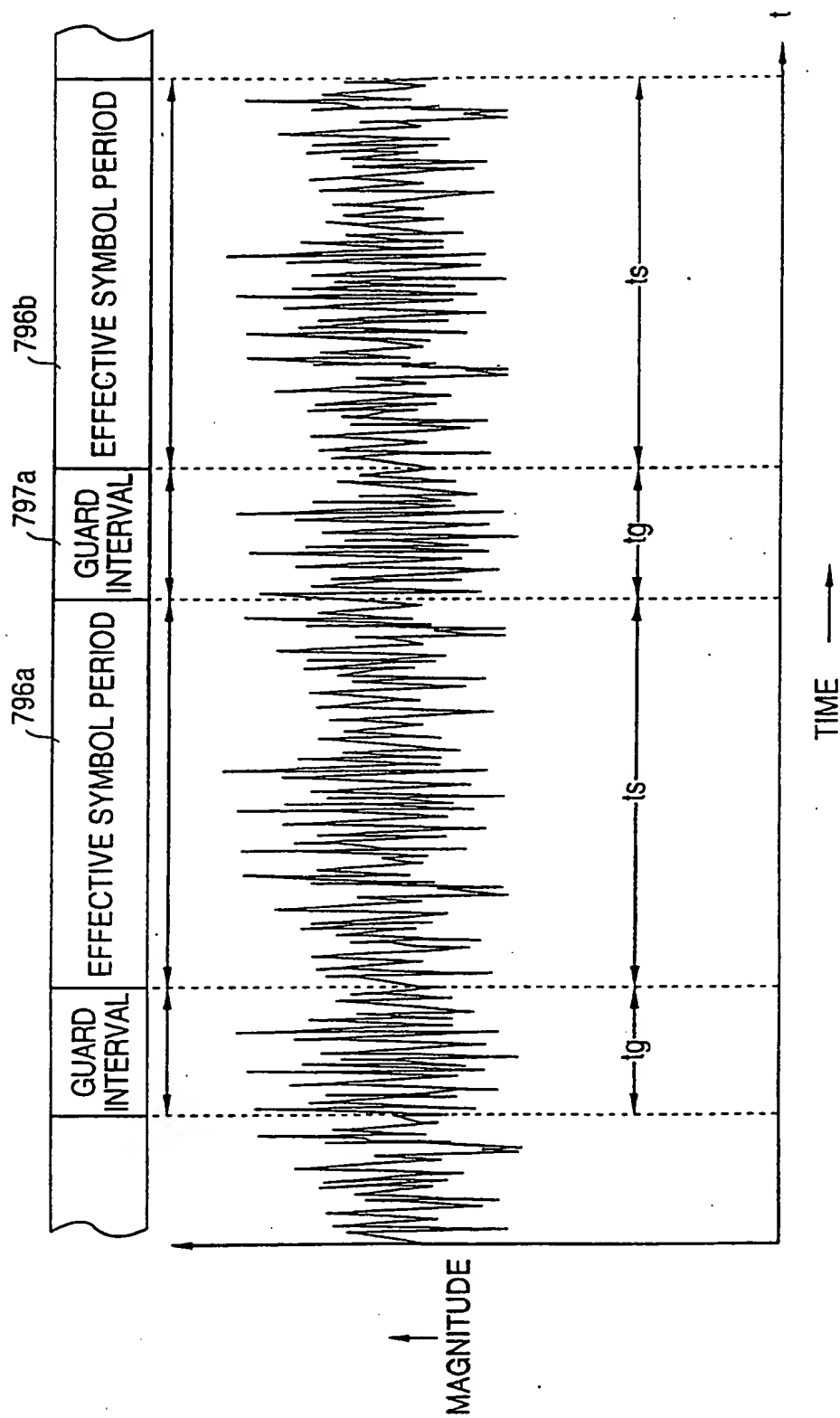


FIG. 130

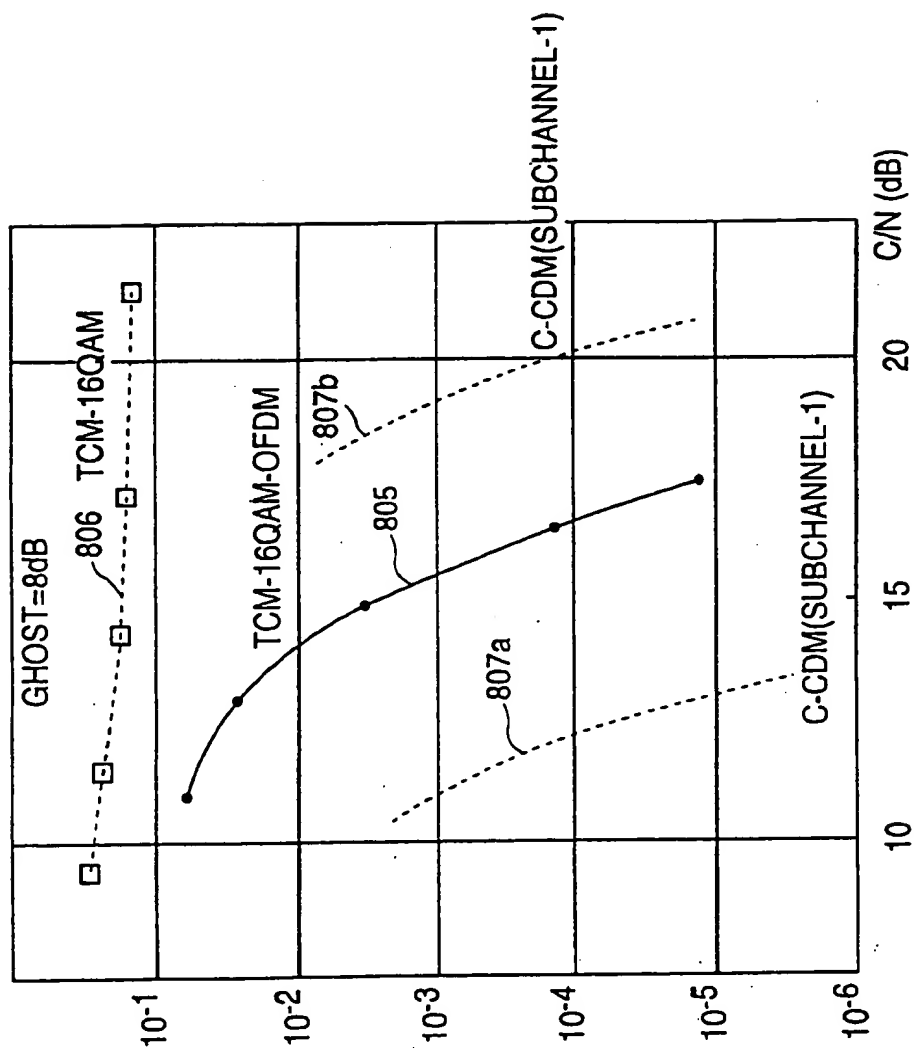
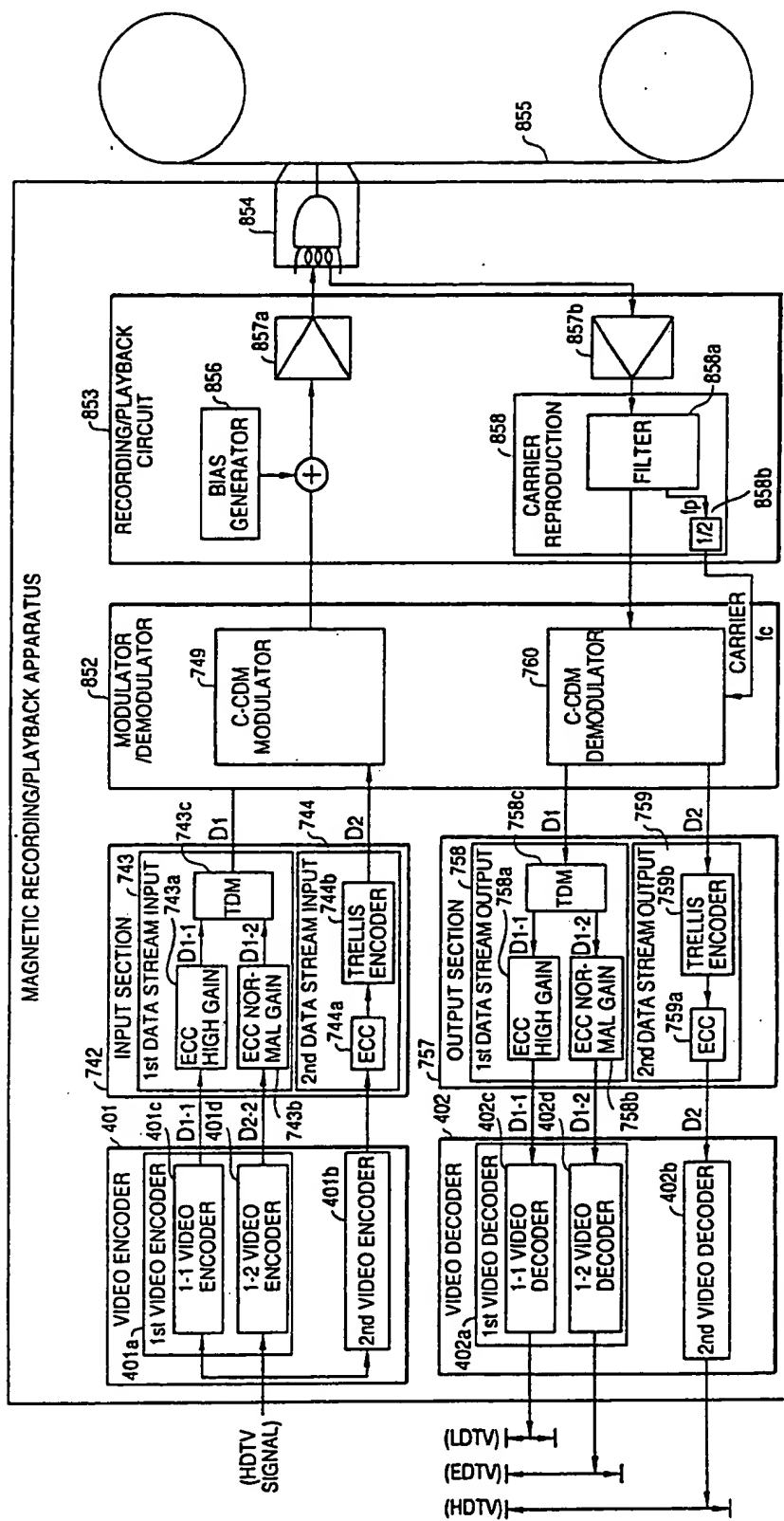


FIG. 131



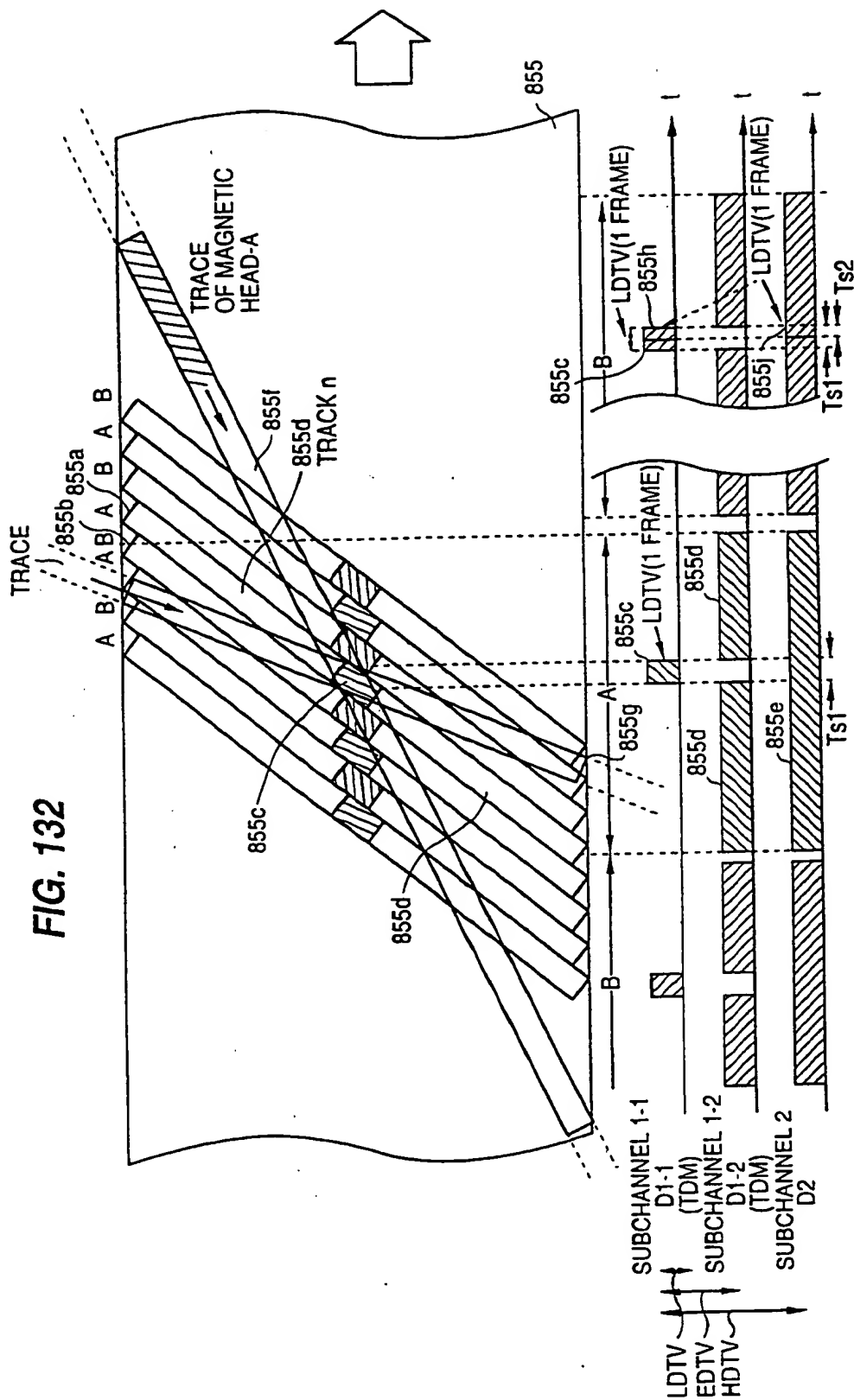


FIG. 133

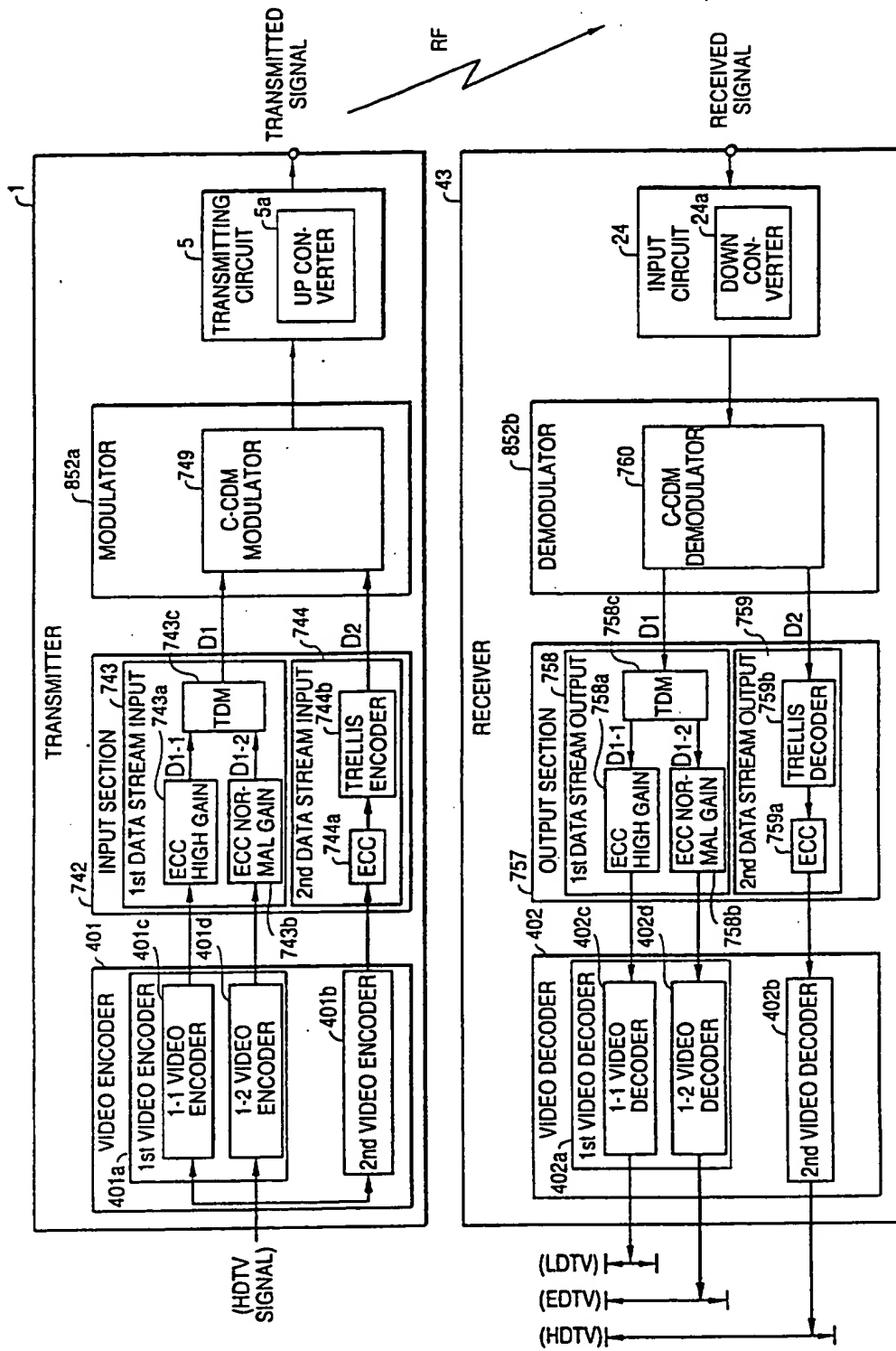


FIG. 134

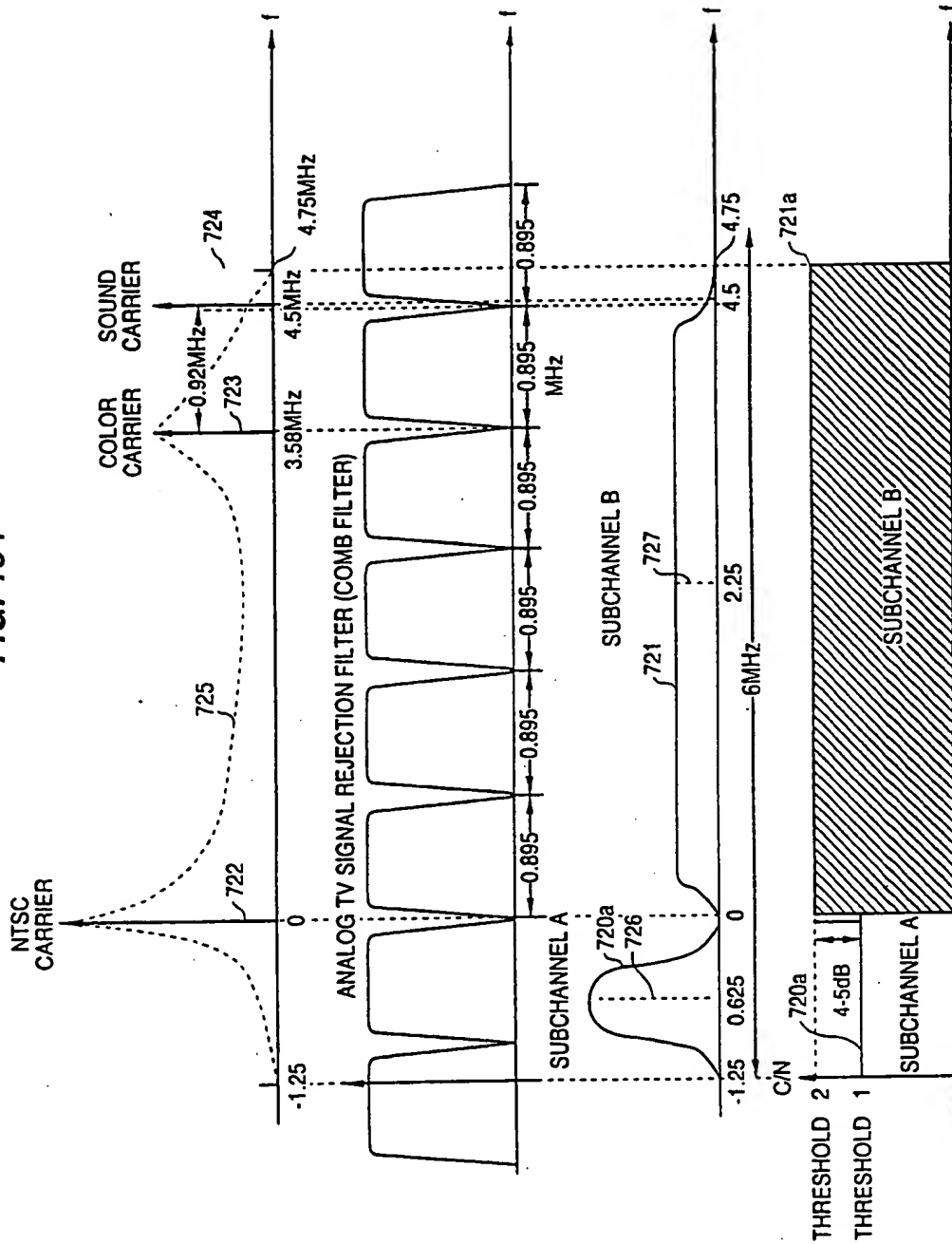


FIG. 135

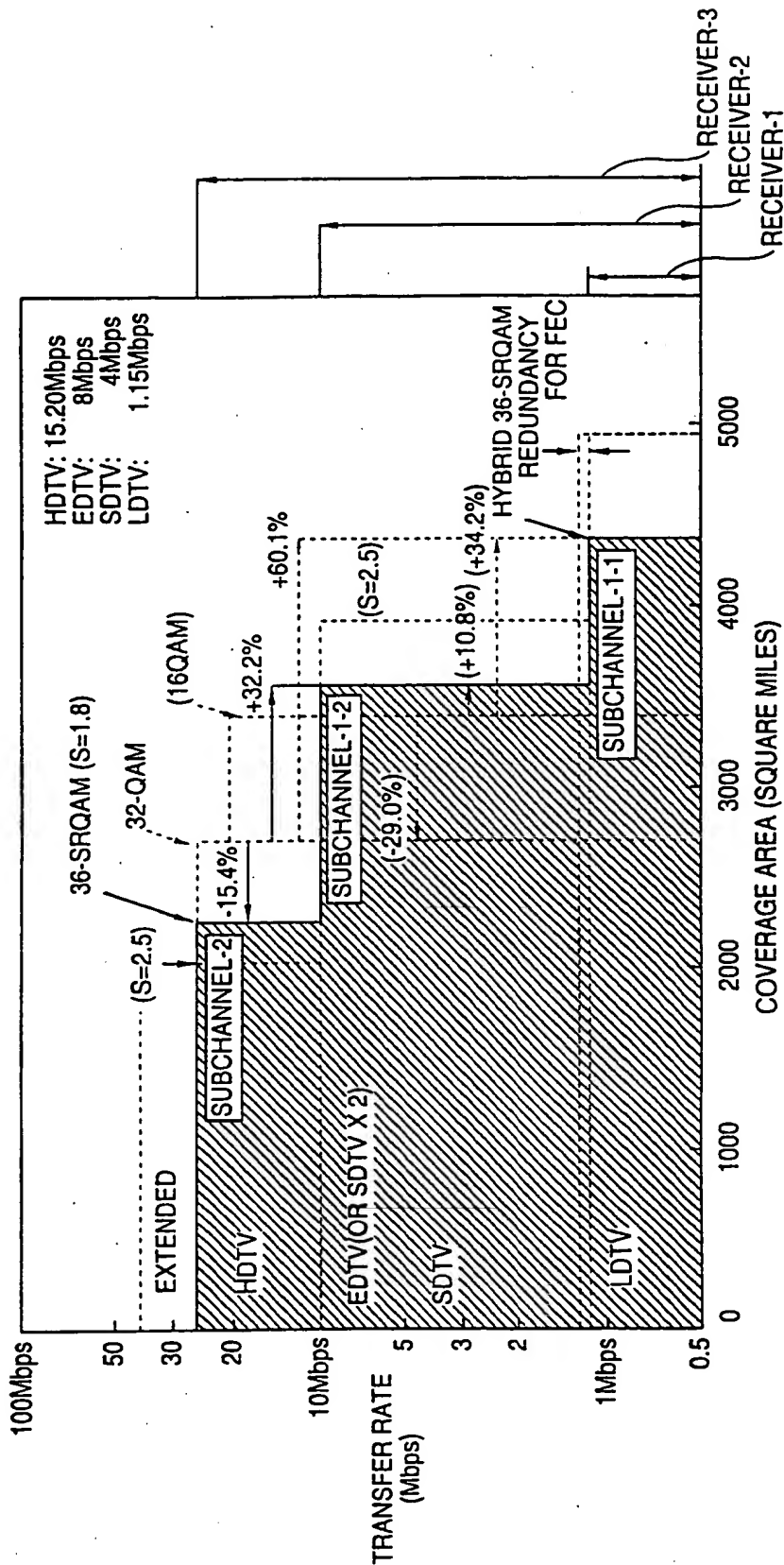


FIG. 136

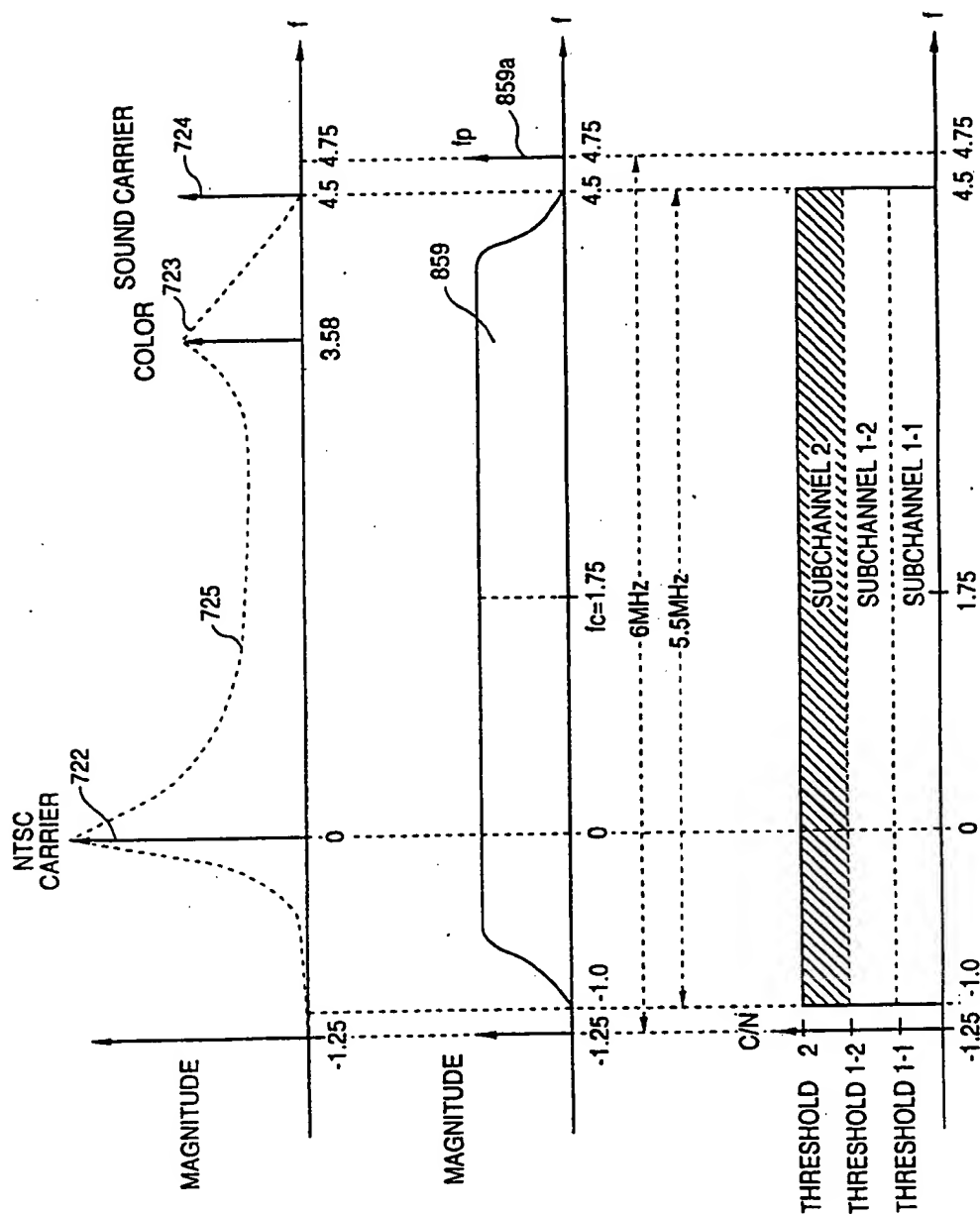


FIG. 137

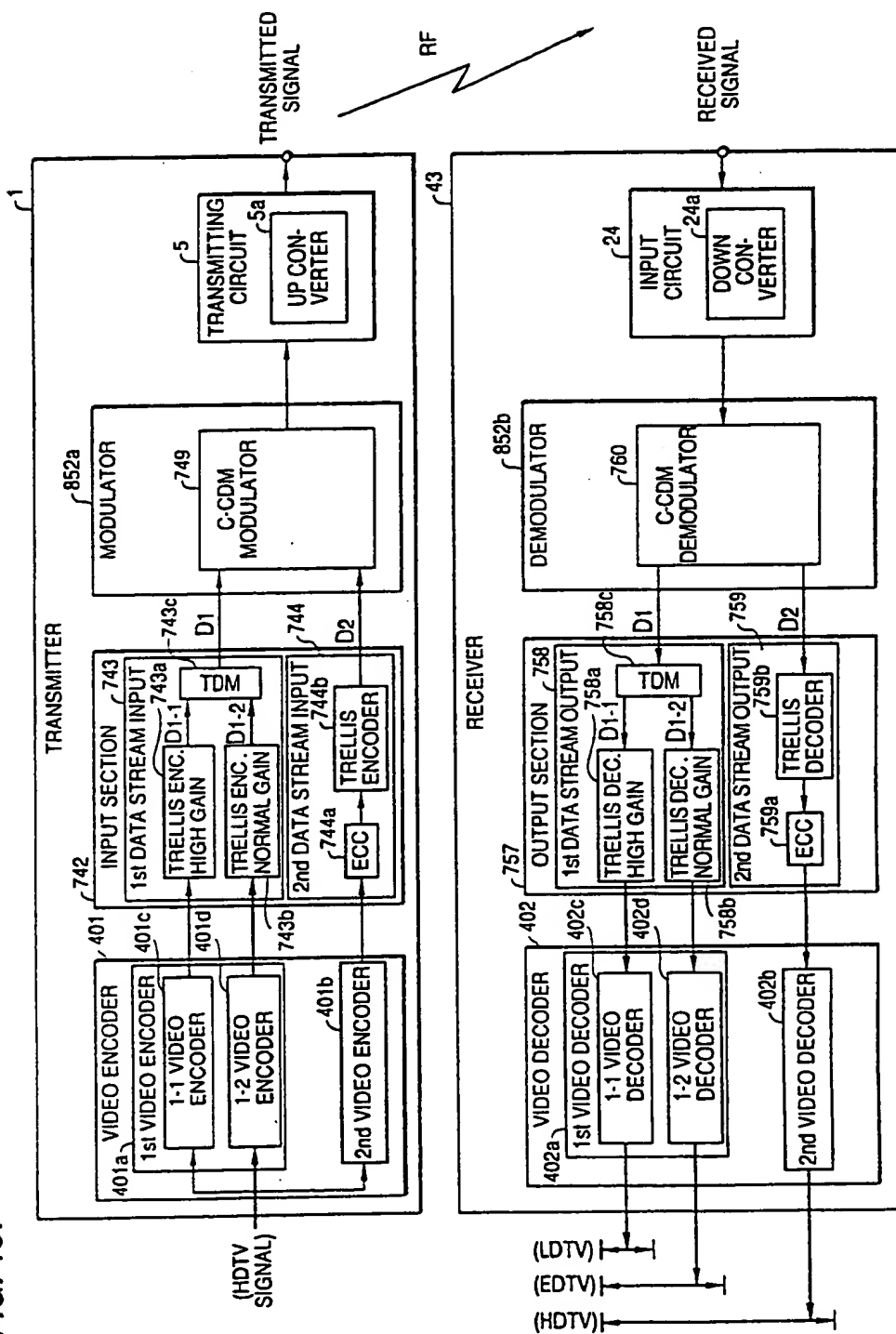


FIG. 138

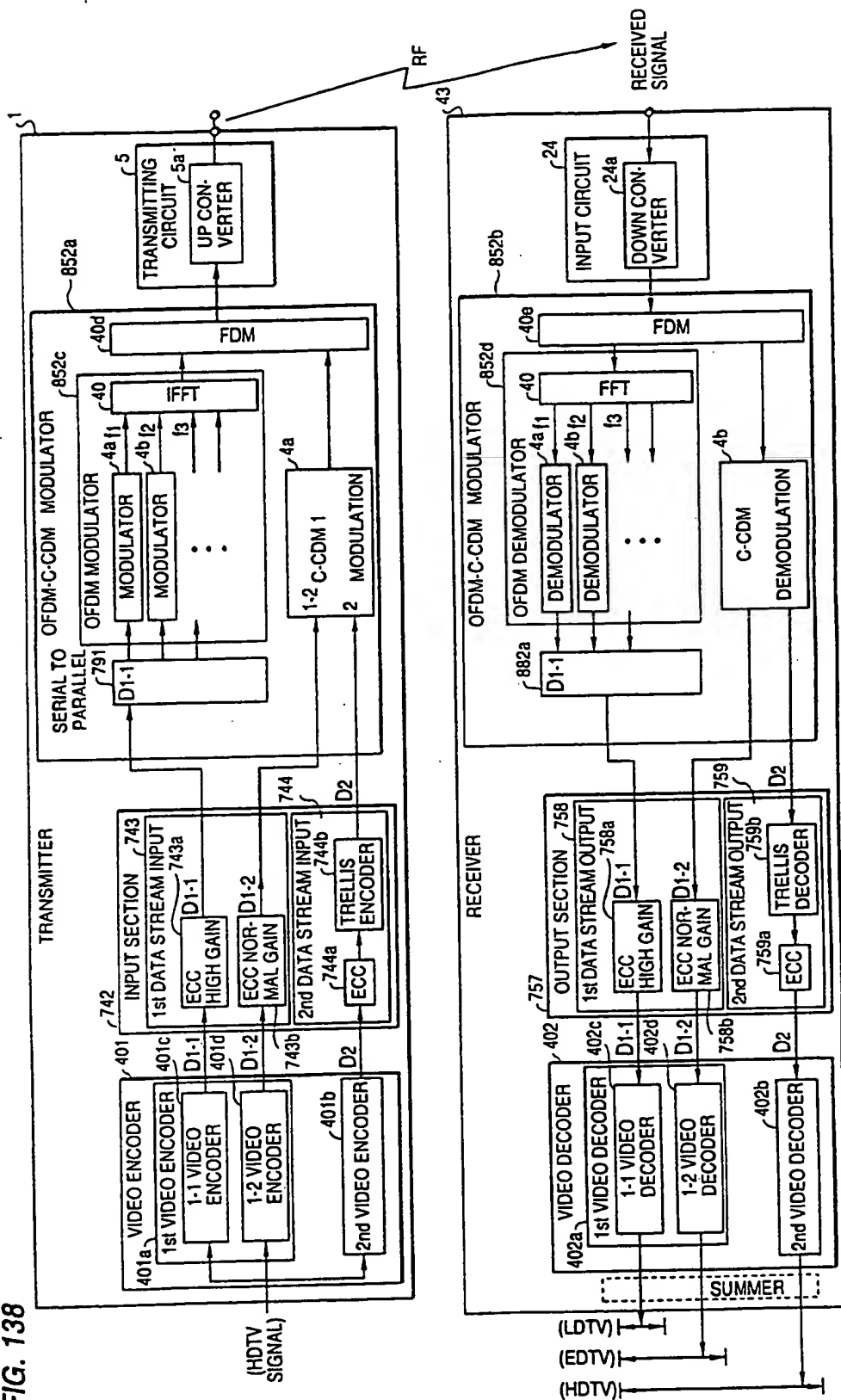
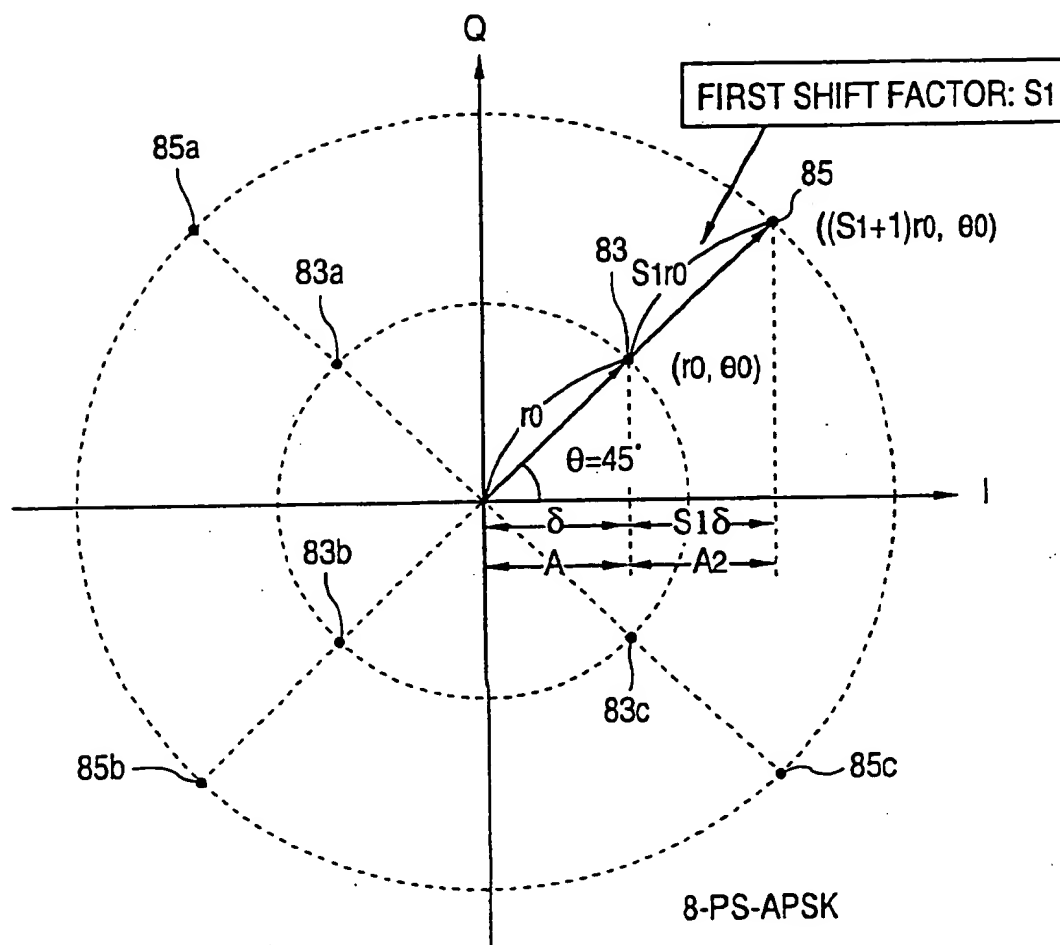


FIG. 139



006007 100600

FIG. 140

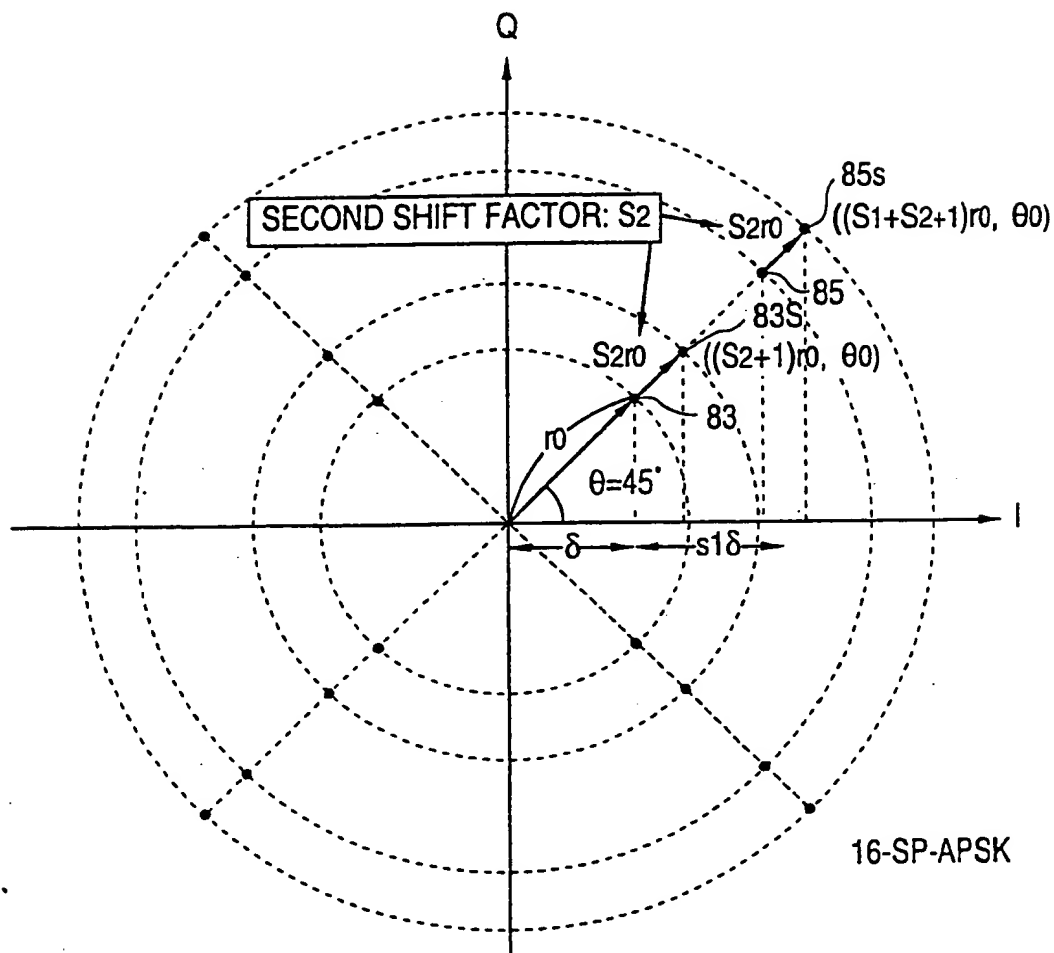


FIG. 141

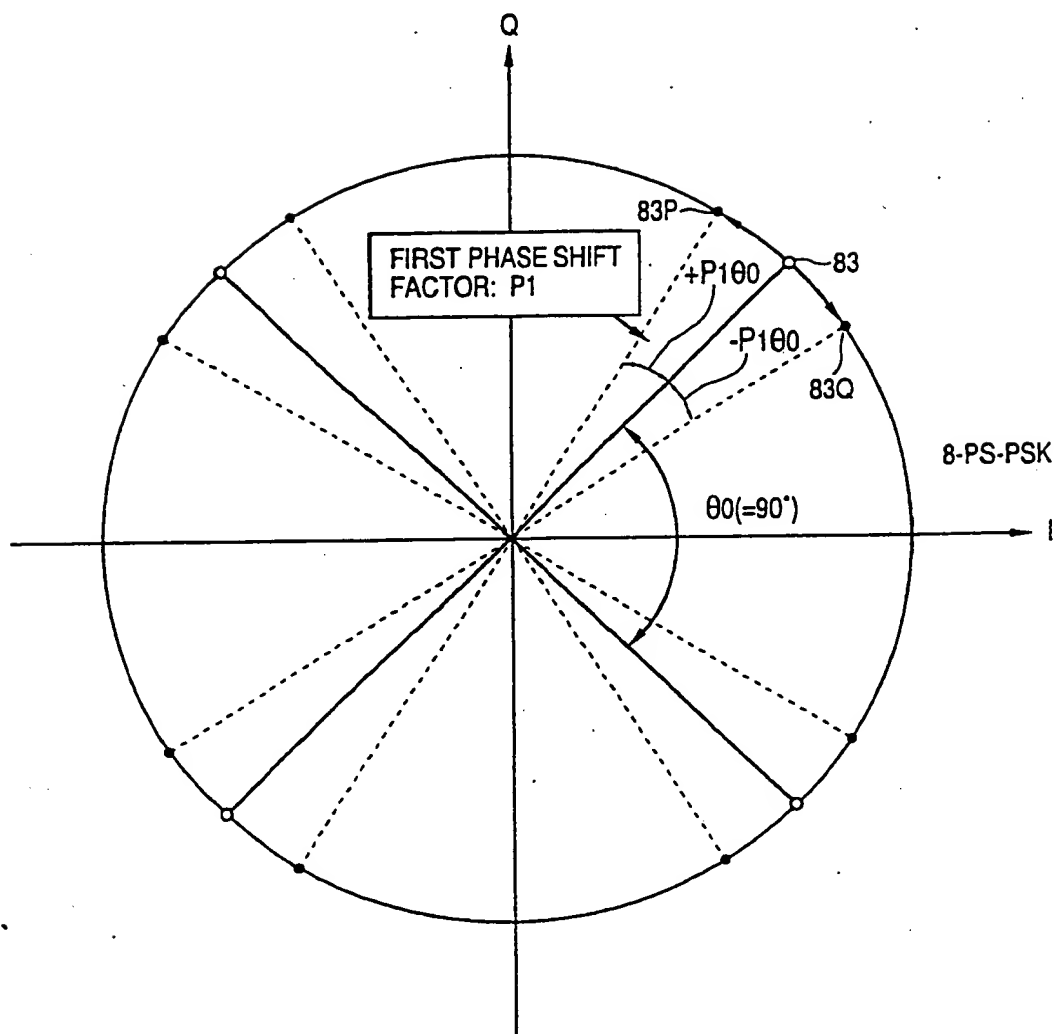
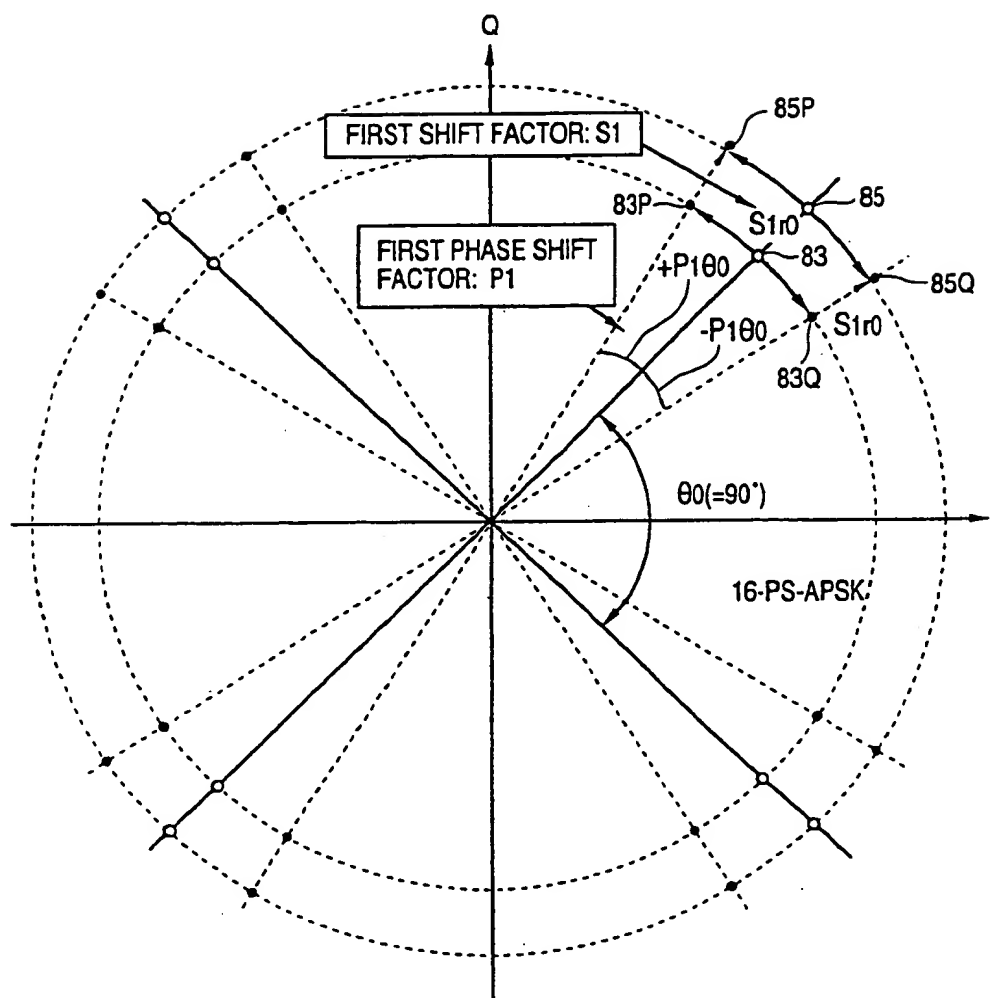
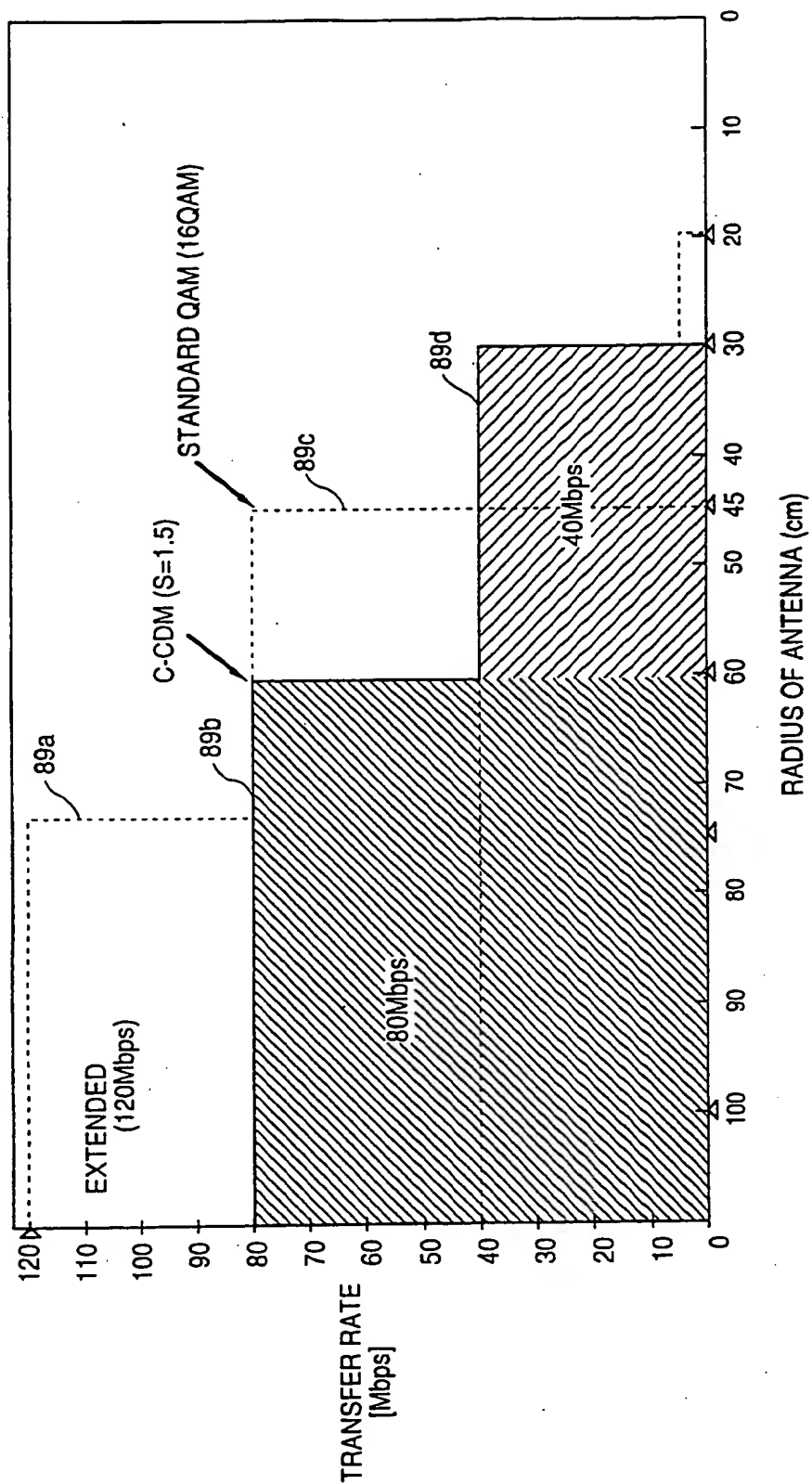


FIG. 142



000001 100000

FIG. 143



The diagram illustrates a video transmission system, divided into a Transmitter (left) and a Receiver (right).

**Transmitter Section:**

- Input Section (743):** Receives an (HDTV SIGNAL). It includes a 1st DATA STREAM INPUT (743a) and a 2nd DATA STREAM INPUT (744b). The 1st input passes through an ECC (743c), HIGH GAIN (743d), and TDM (743e) blocks. The 2nd input passes through an ECC (744a), MAL GAIN (744c), and TDM (744d) blocks.
- Encoding:** The outputs from the 1st and 2nd data stream inputs are processed by a VIDEO ENCODER (401a) and a 2nd VIDEO ENCODER (401b). The 1st video encoder includes 1-1 VIDEO ENCODER (401c) and 1-2 VIDEO ENCODER (401d) blocks. The 2nd video encoder includes 2-1 VIDEO ENCODER (401e) and 2-2 VIDEO ENCODER (401f) blocks.
- Serial to Parallel Conversion:** The encoded streams are converted from serial to parallel by a D2 SERIAL TO PARALLEL block (791a).
- Modulation:** The parallel streams are processed by a WEIGHTED OFDM-MODULATOR (4). This block includes multiple MOD. blocks (4a1f, 4b1f, 4c1f, 4d1f, 4e1f) and a D/A CONVERTER (4e).
- Transmission:** The modulated signal is sent to a TRANSMIT CIRCUIT (5) via an UP CON-VERTER (5a), which is connected to an RF output.

**Receiver Section:**

- Reception:** The RECEIVER receives a RECEIVED SIGNAL, which is converted by a DOWN CON-VERTER (2a) and an INPUT CIRCUIT (24).
- Demodulation:** The signal is processed by a WEIGHTED OFDM-DEMODULATOR (45). This block includes multiple DEMOD. blocks (45a1f, 45b1f, 45c1f, 45d1f, 45e1f) and an A/D CONVERTER (40c).
- Parallel to Serial Conversion:** The demodulated streams are converted from parallel to serial by a D2 SERIAL TO PARALLEL block (791a).
- Decoding:** The serial streams are processed by a VIDEO DECODER (402a) and a 2nd VIDEO DECODER (402b). The 1st video decoder includes 1-1 VIDEO DECODER (402c) and 1-2 VIDEO DECODER (402d) blocks. The 2nd video decoder includes 2-1 VIDEO DECODER (402e) and 2-2 VIDEO DECODER (402f) blocks.
- Output Section (758):** The decoded streams are processed by an ECC (758a), HIGH GAIN (758b), and TDM (758c) blocks. The 2nd data stream output (759b) is processed by an ECC (759a), MAL GAIN (759c), and TDM (759d) blocks.
- Summing:** The outputs from the 1st and 2nd data stream outputs are combined in a SUMMER block (757).
- Output:** The summed signal is sent to the output section (758), which includes a 1st DATA STREAM OUTPUT (758a) and a 2nd DATA STREAM OUTPUT (759b).

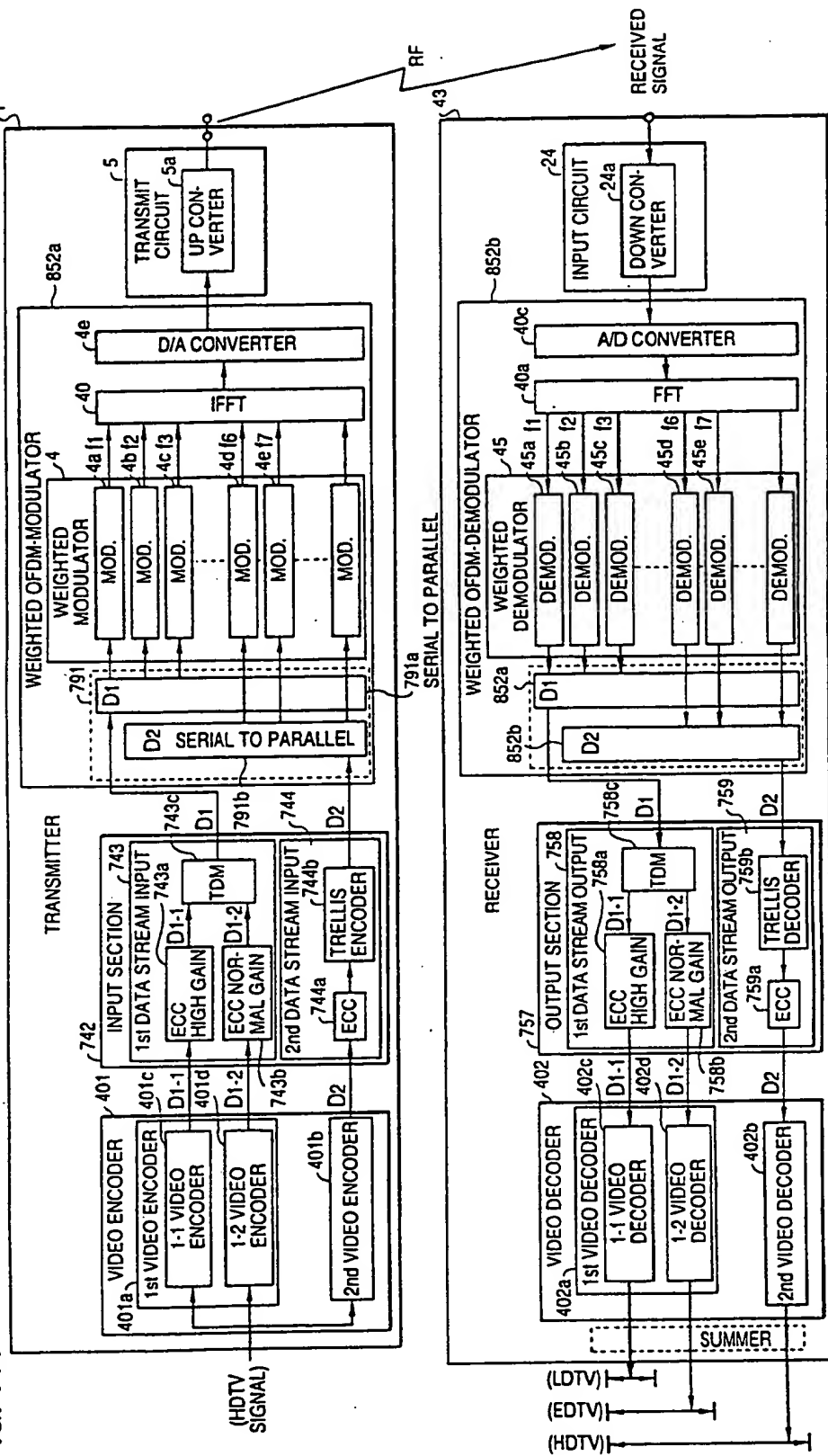


FIG. 145(a)

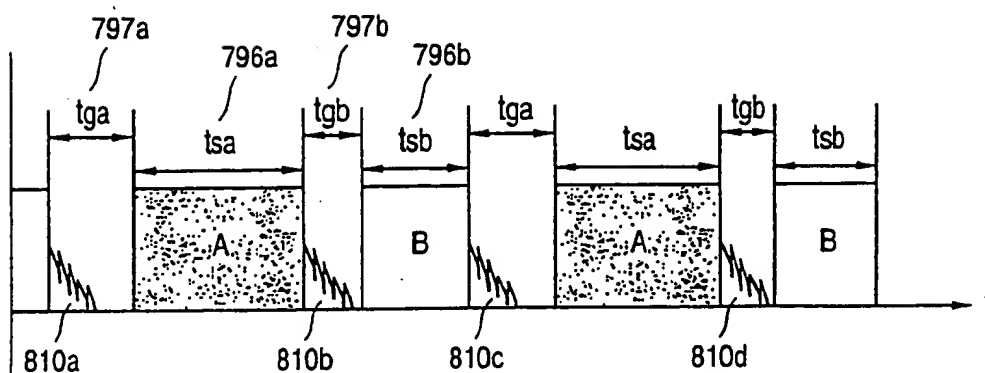


FIG. 145(b)

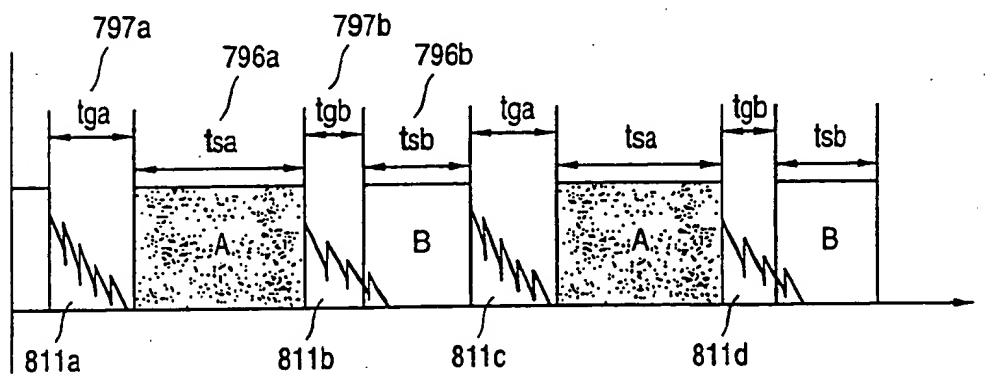




FIG. 147

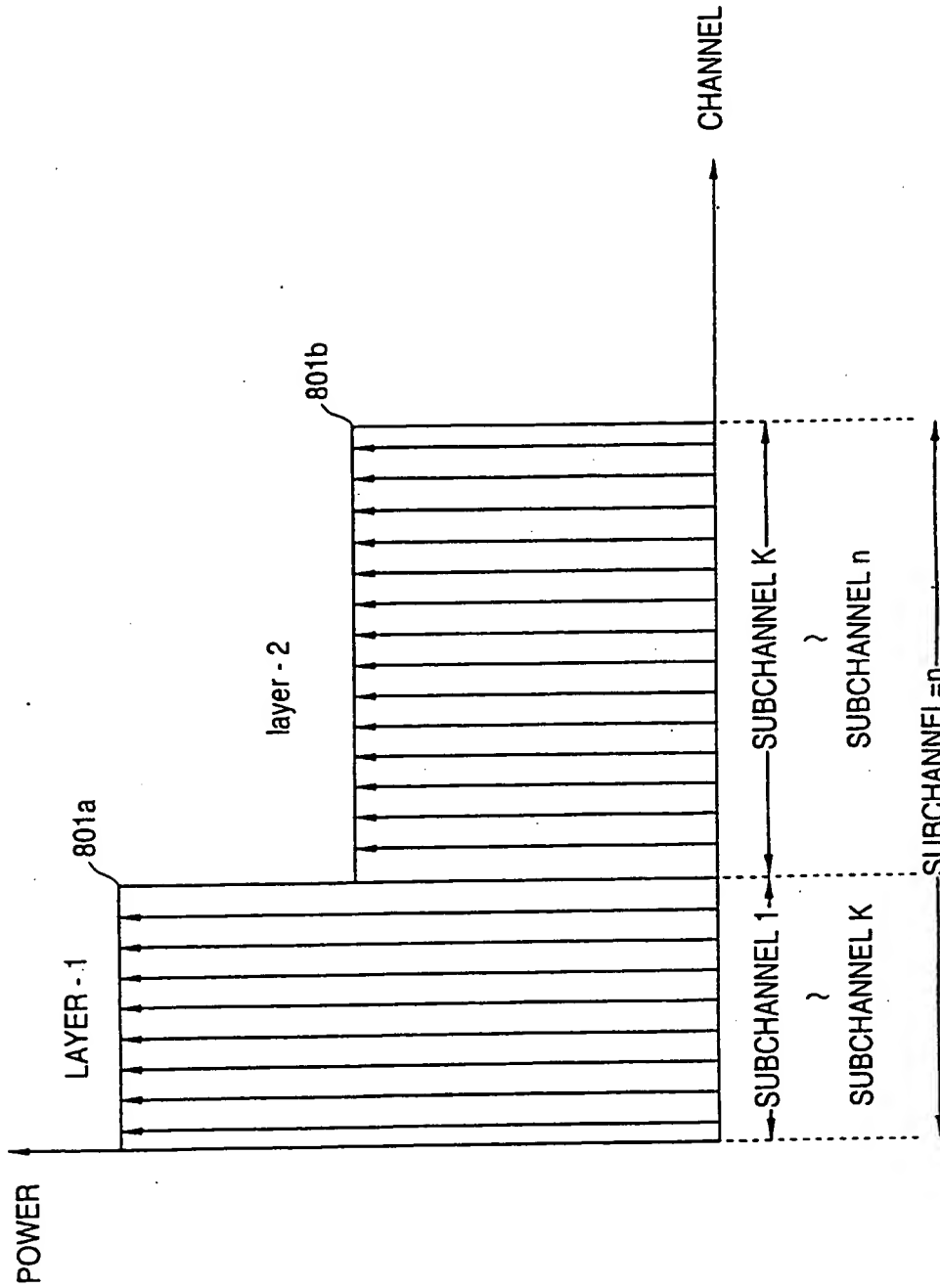
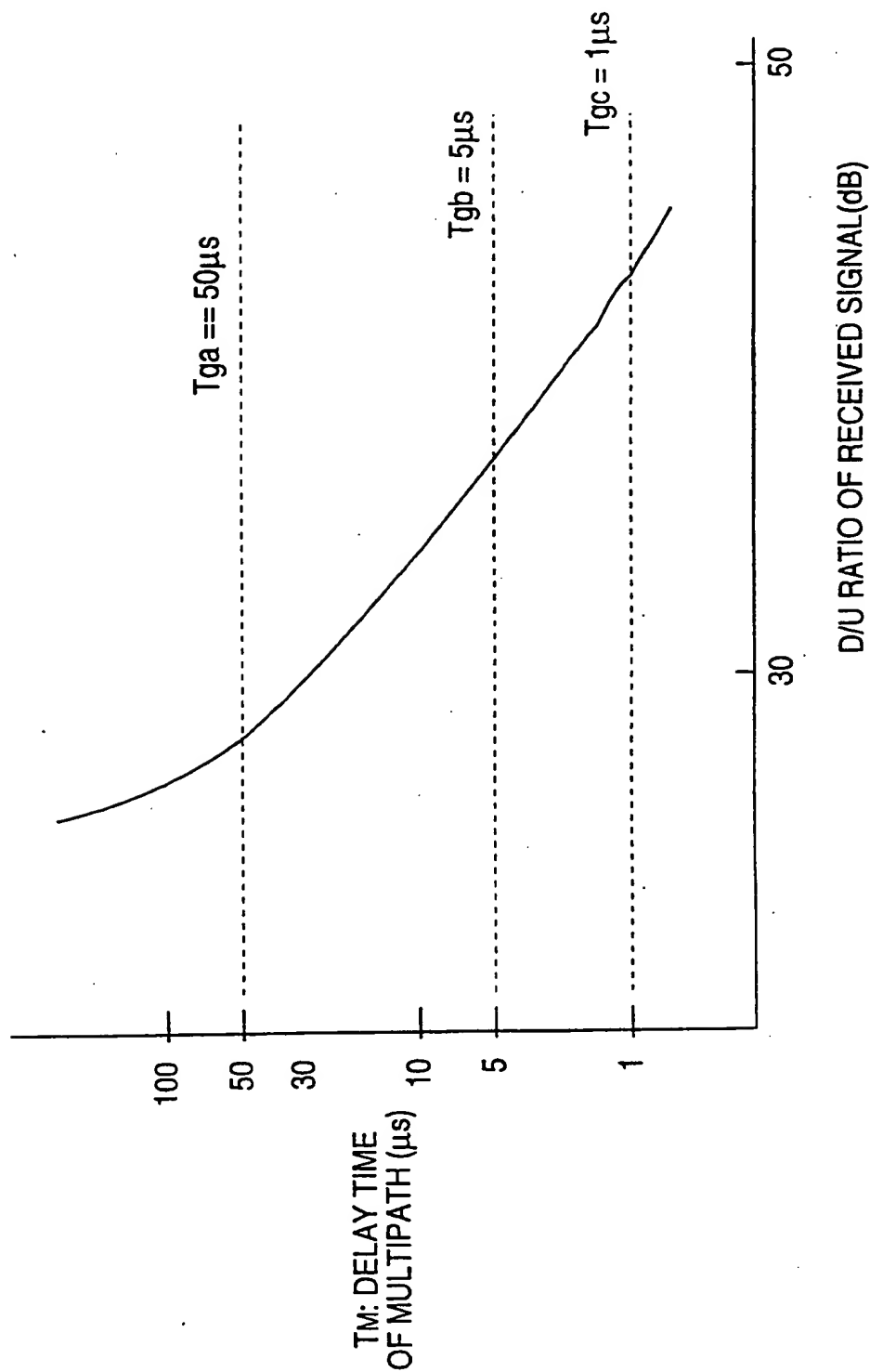
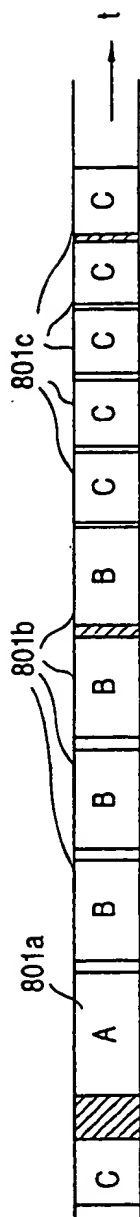


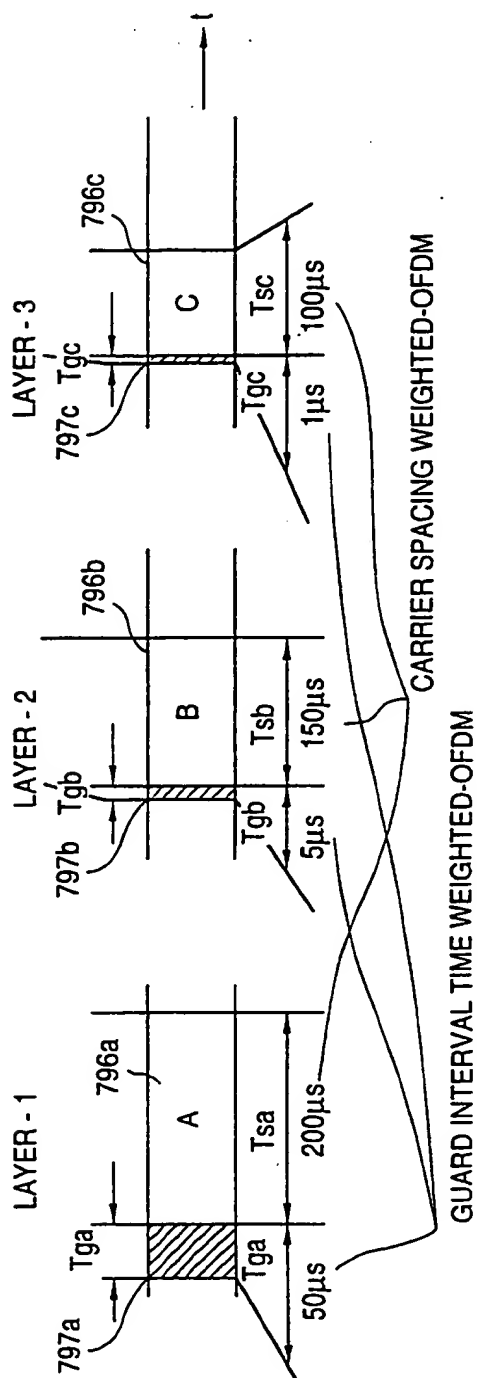
FIG. 148



**FIG. 149(a)**



**FIG. 149(b)**



**FIG. 149(c)**

FIG. 150

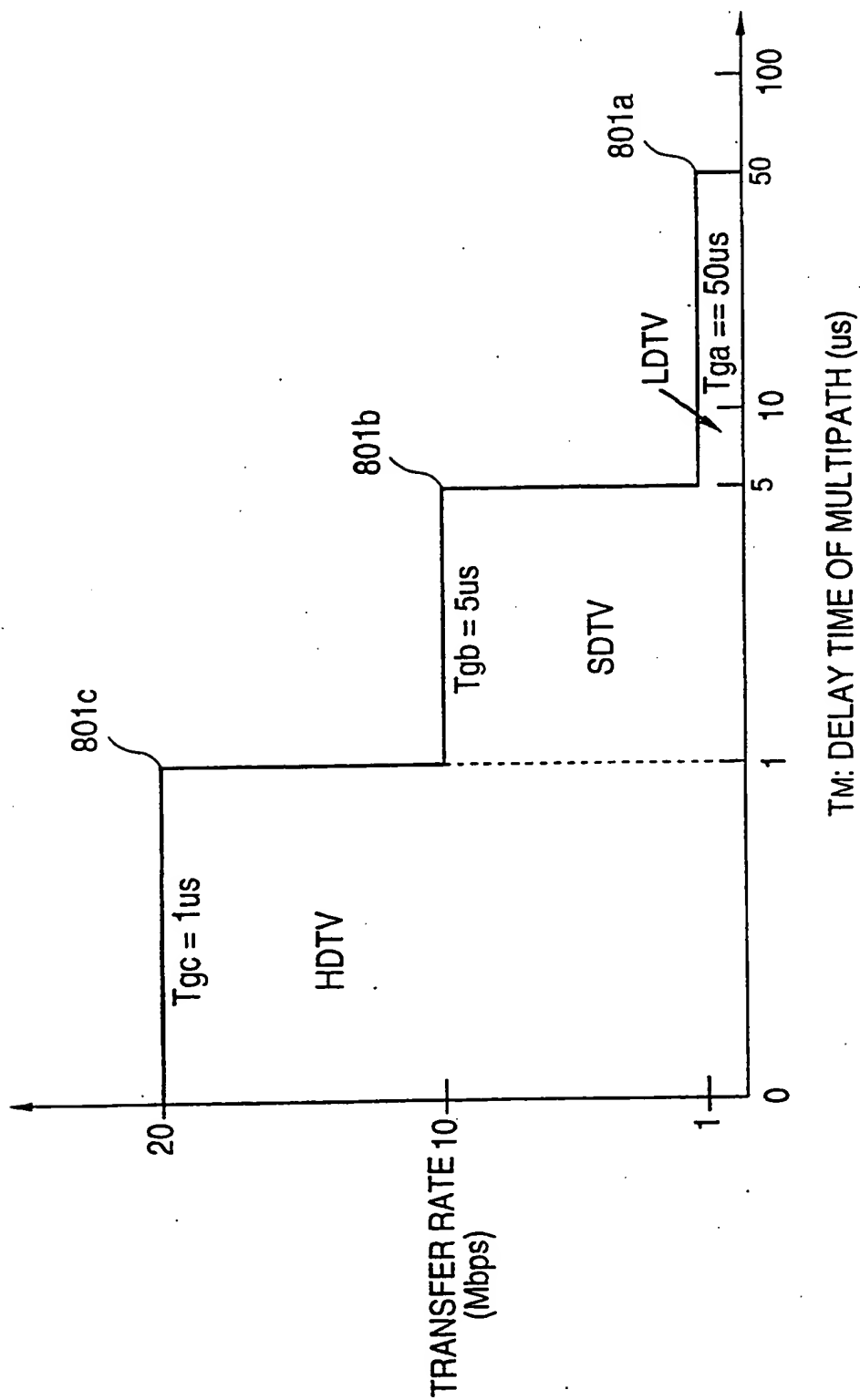


FIG. 151

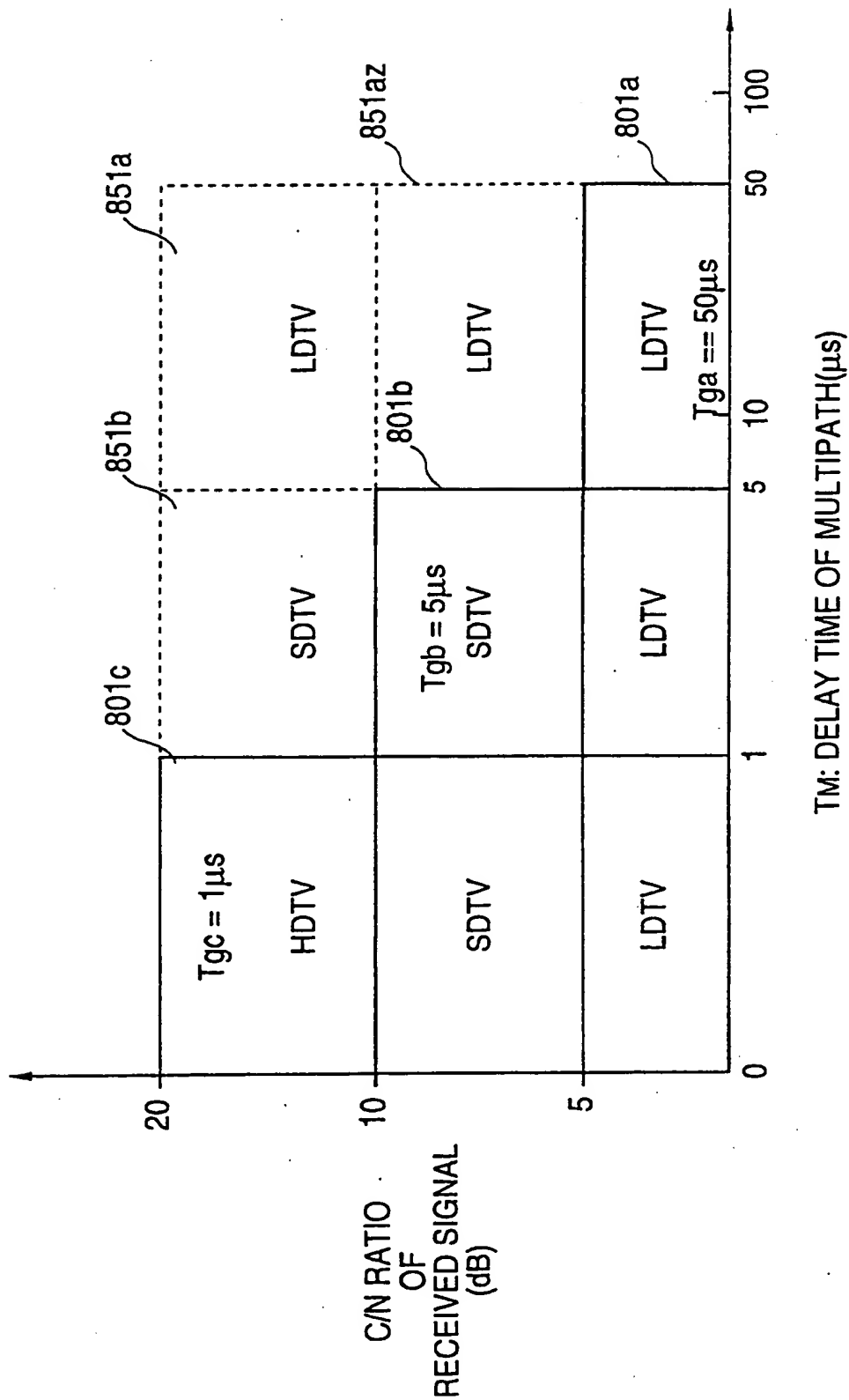


FIG. 152

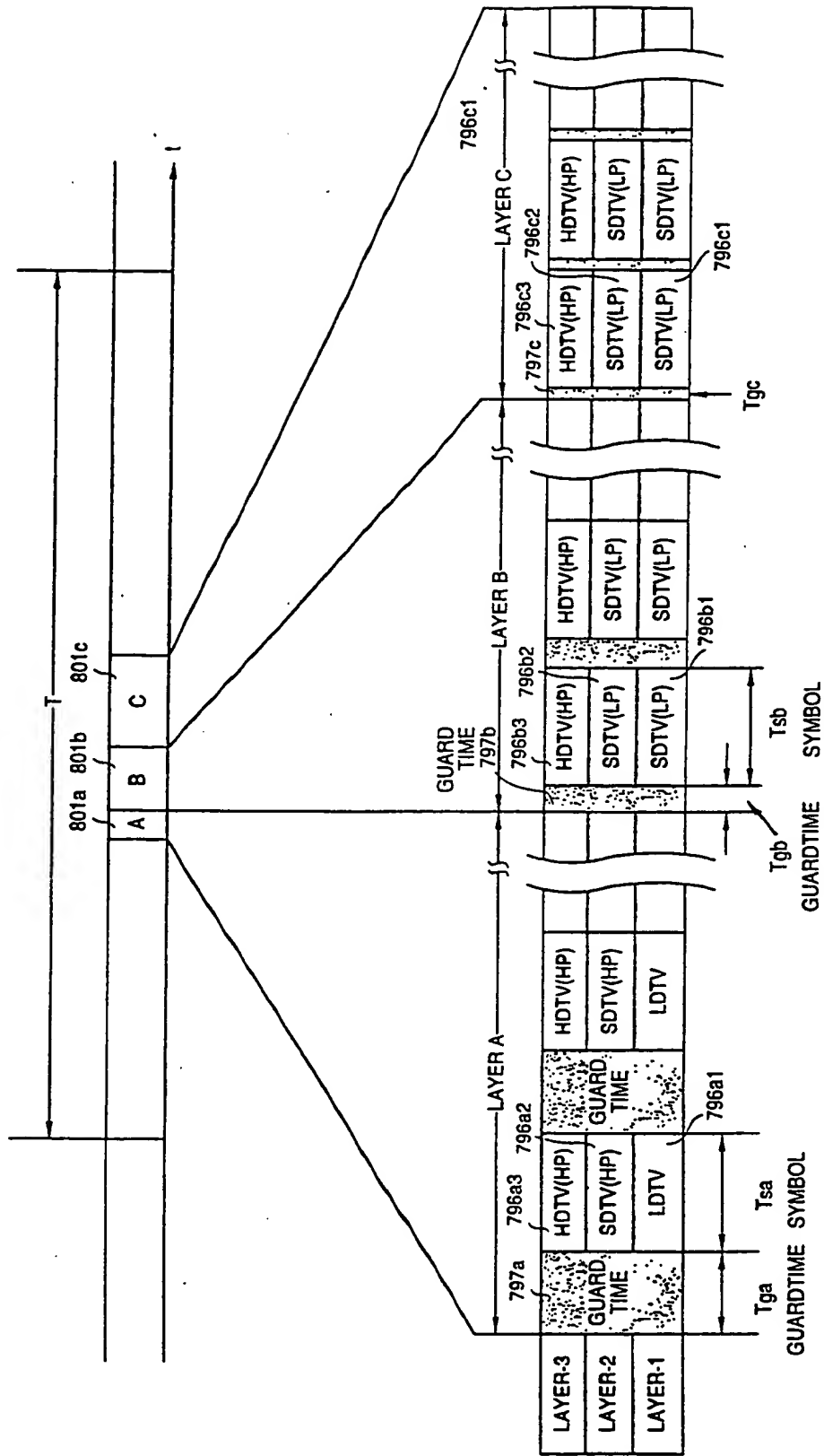
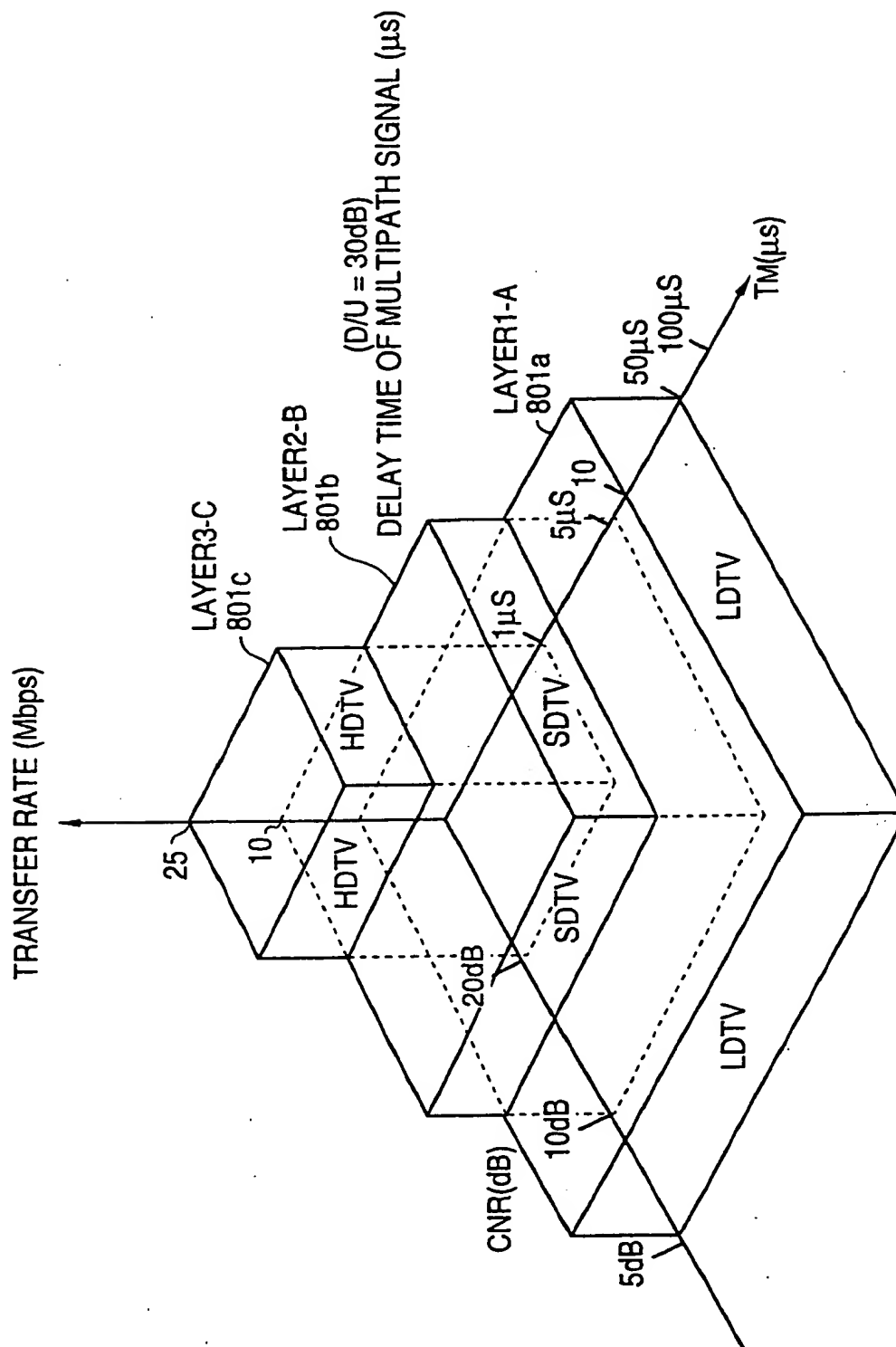


FIG. 153



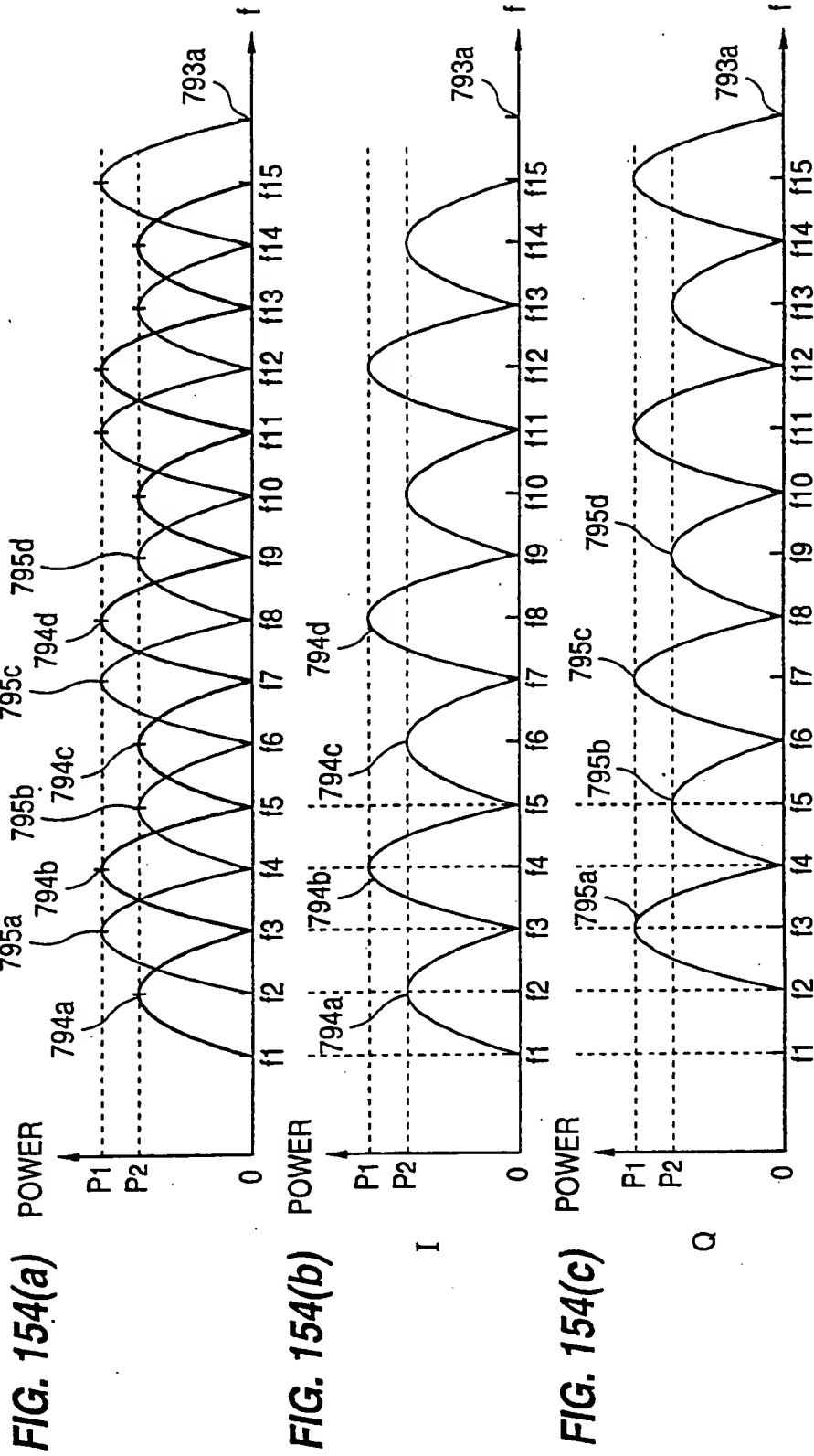


FIG. 155

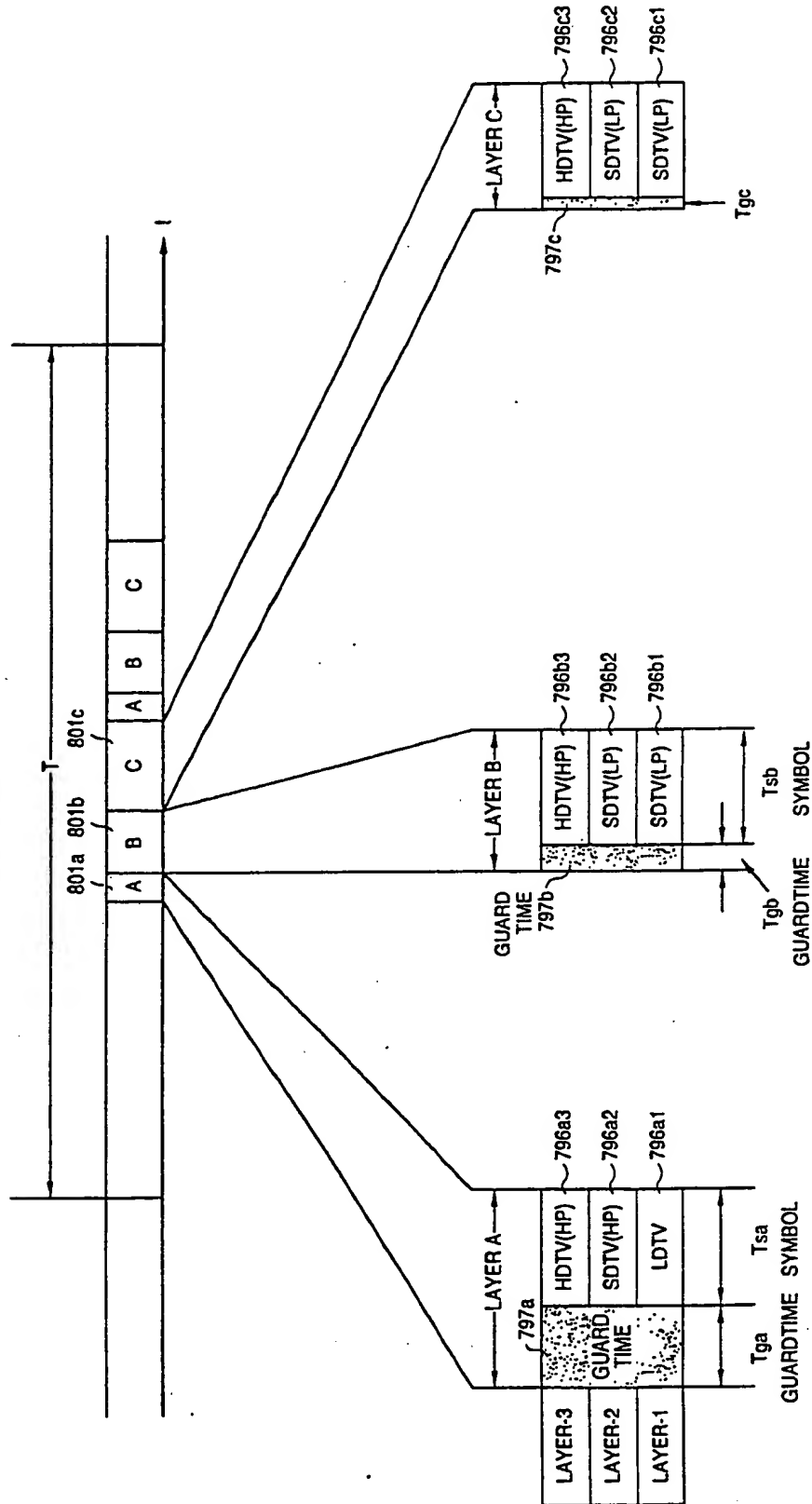


FIG. 156

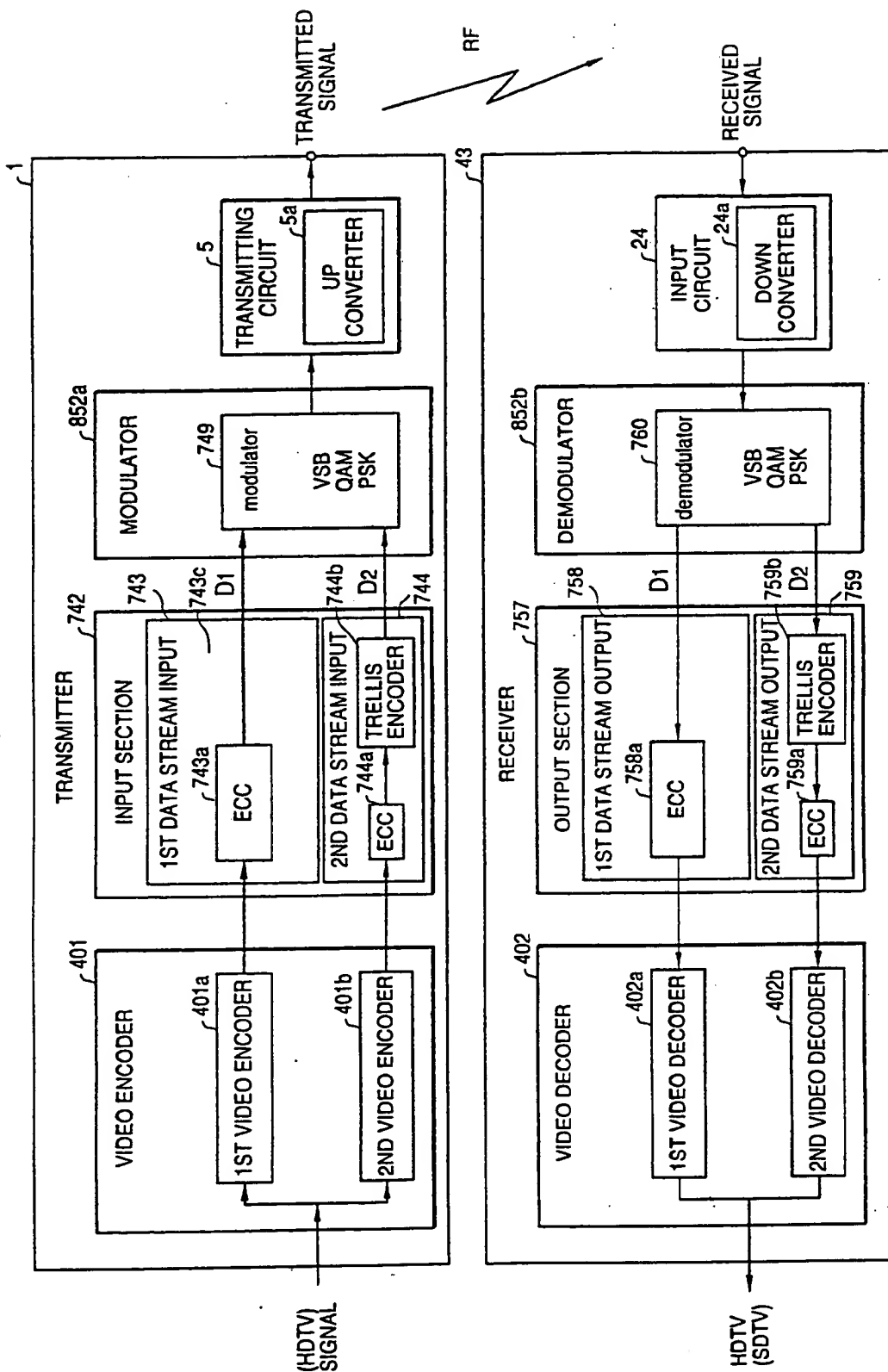


FIG. 157

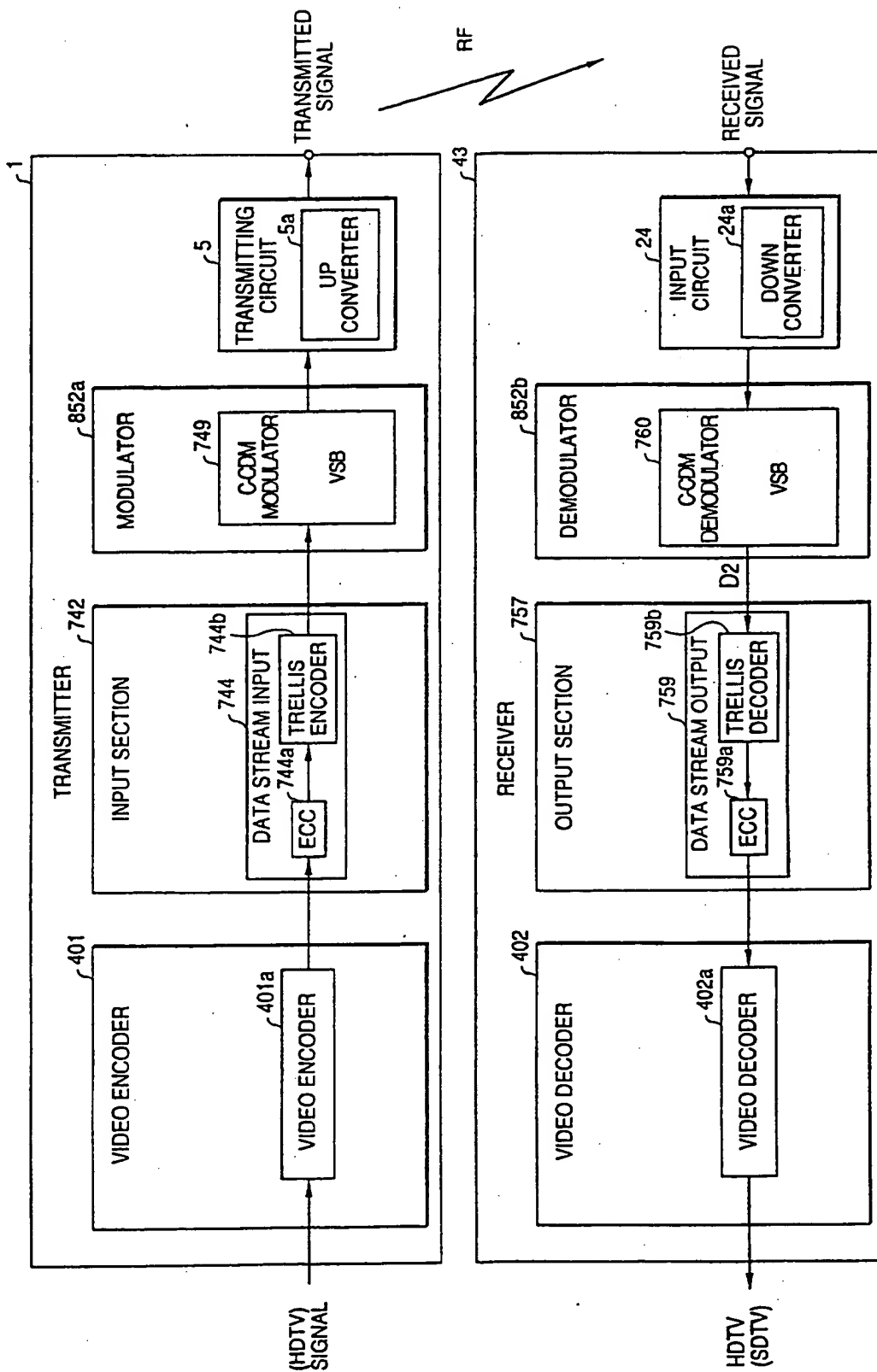
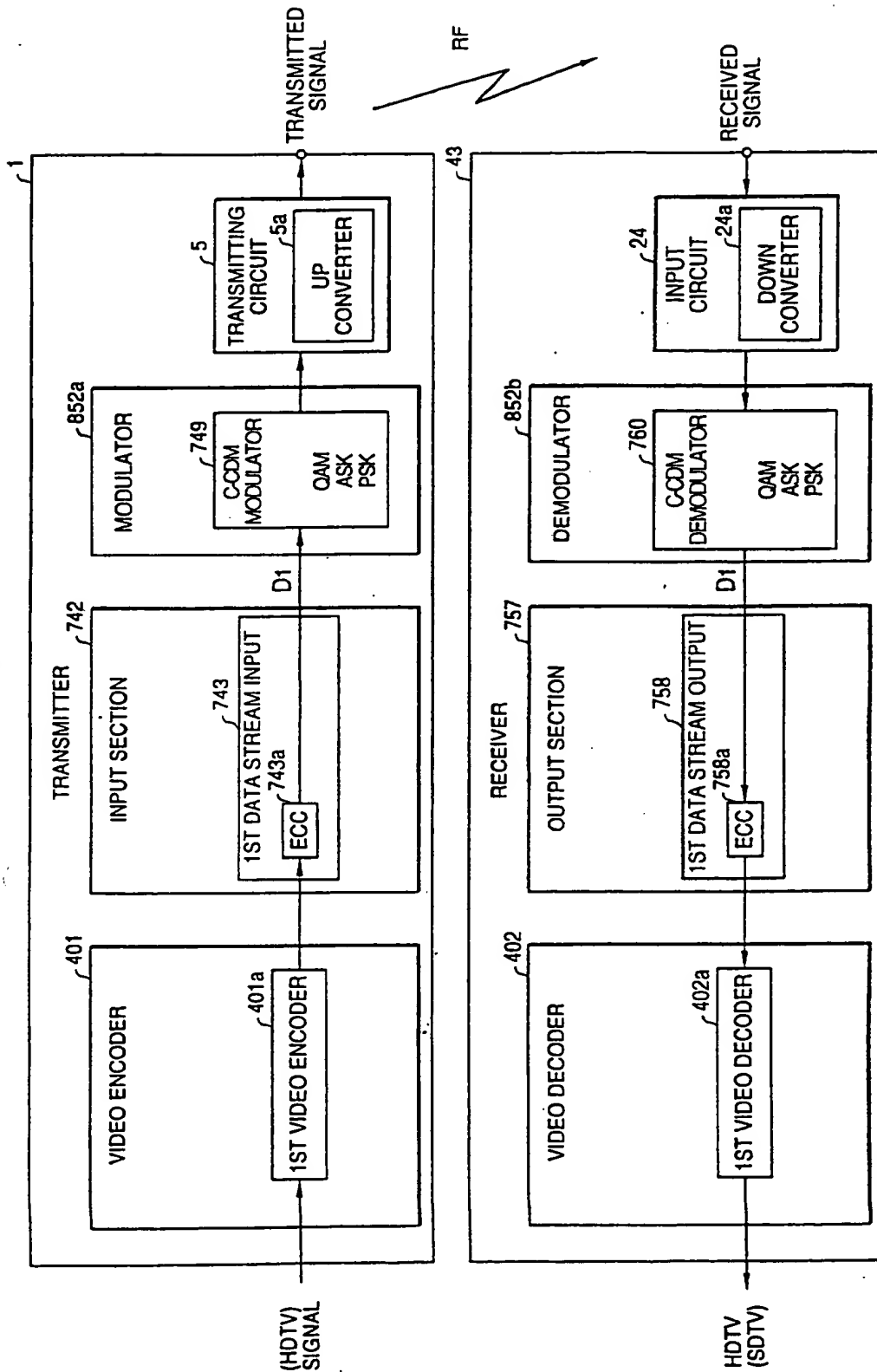


FIG. 158



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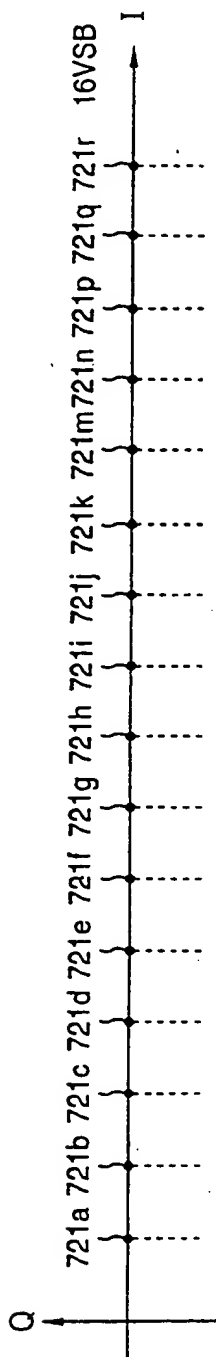


FIG. 159(a)

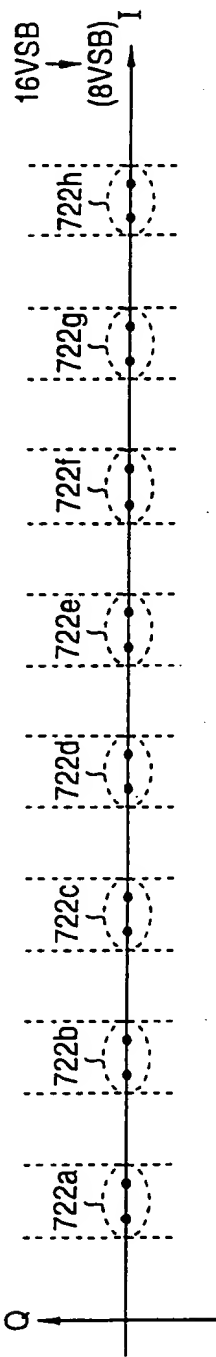


FIG. 159(b)

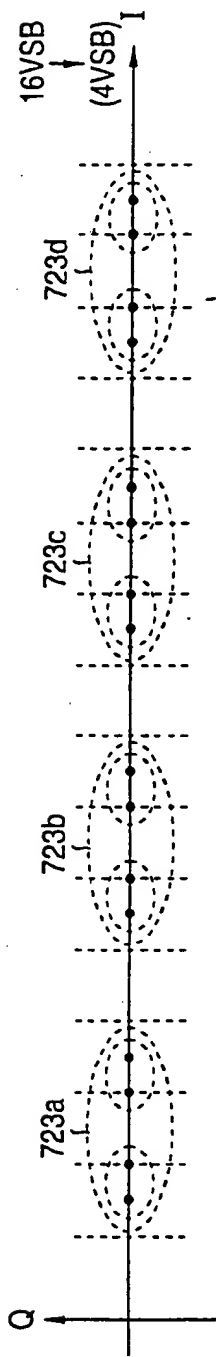


FIG. 159(c)

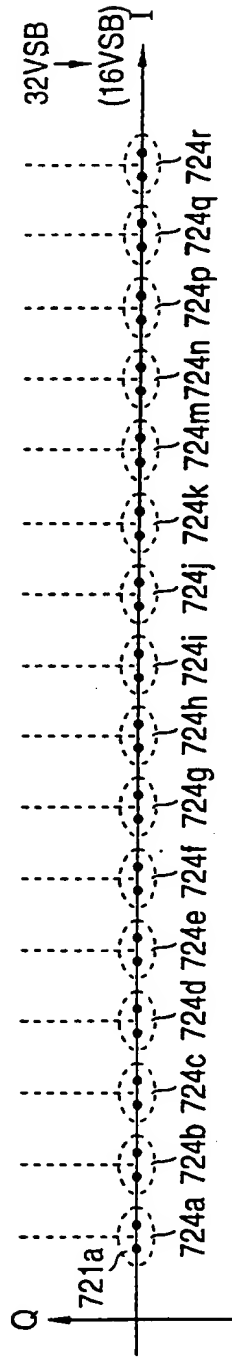


FIG. 159(d)



FIG. 161

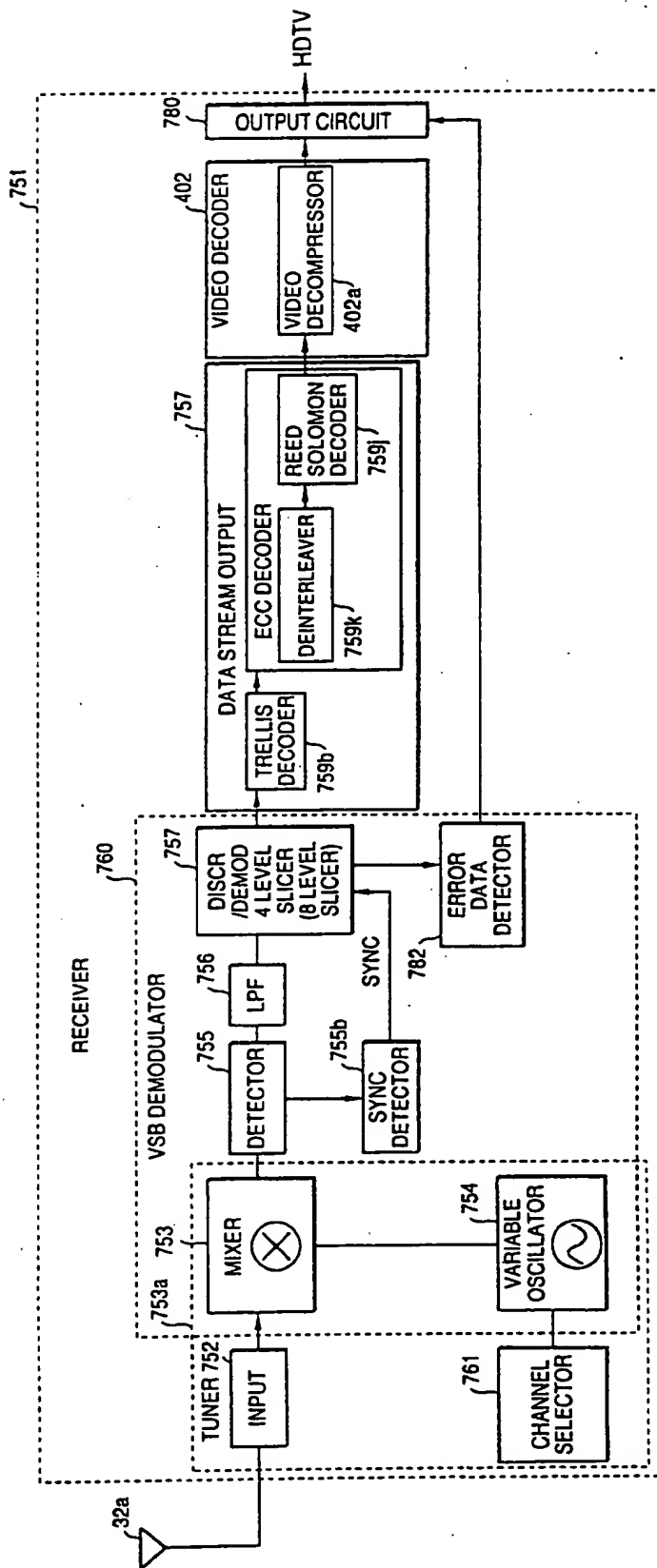


FIG. 162

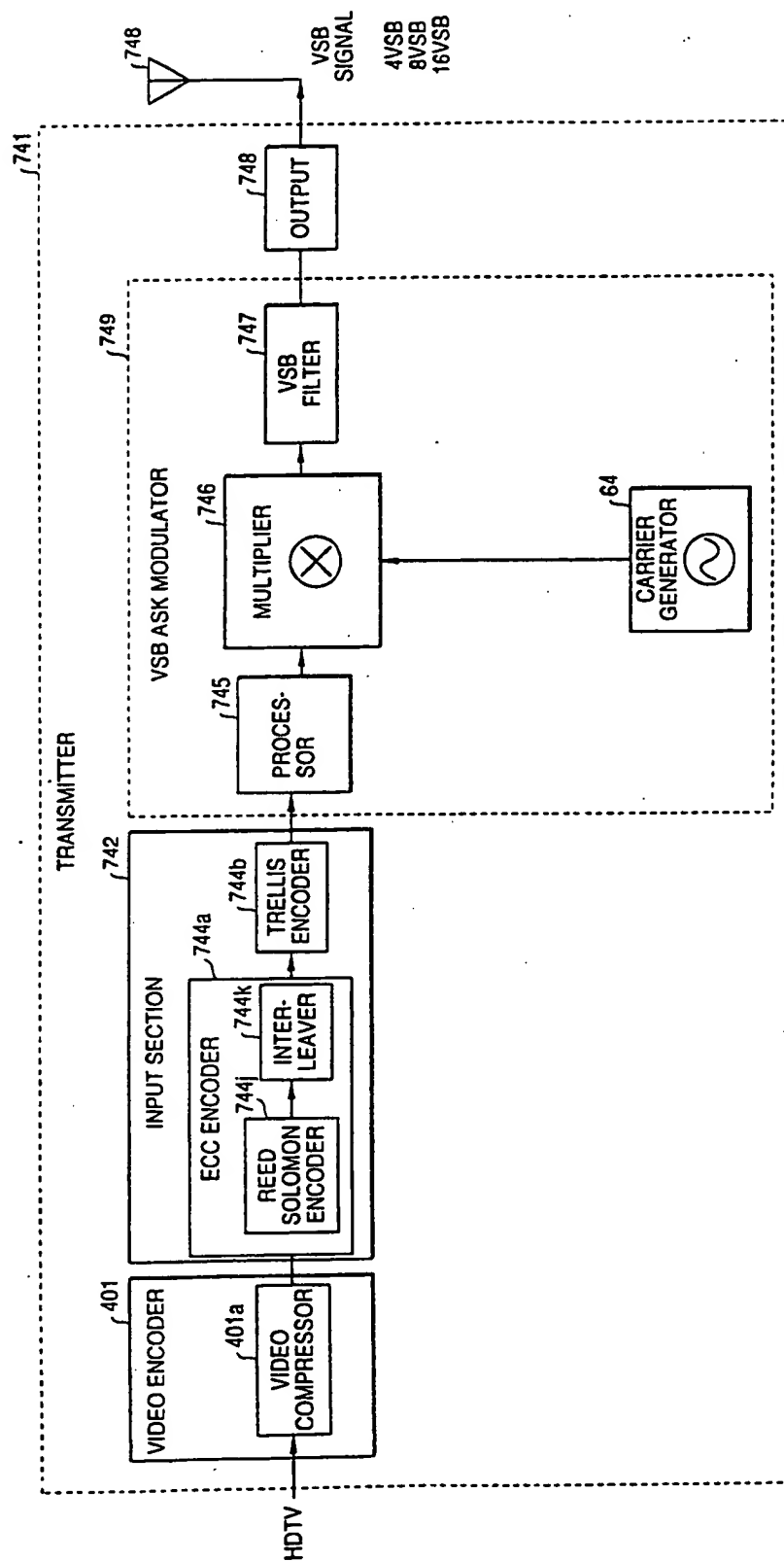
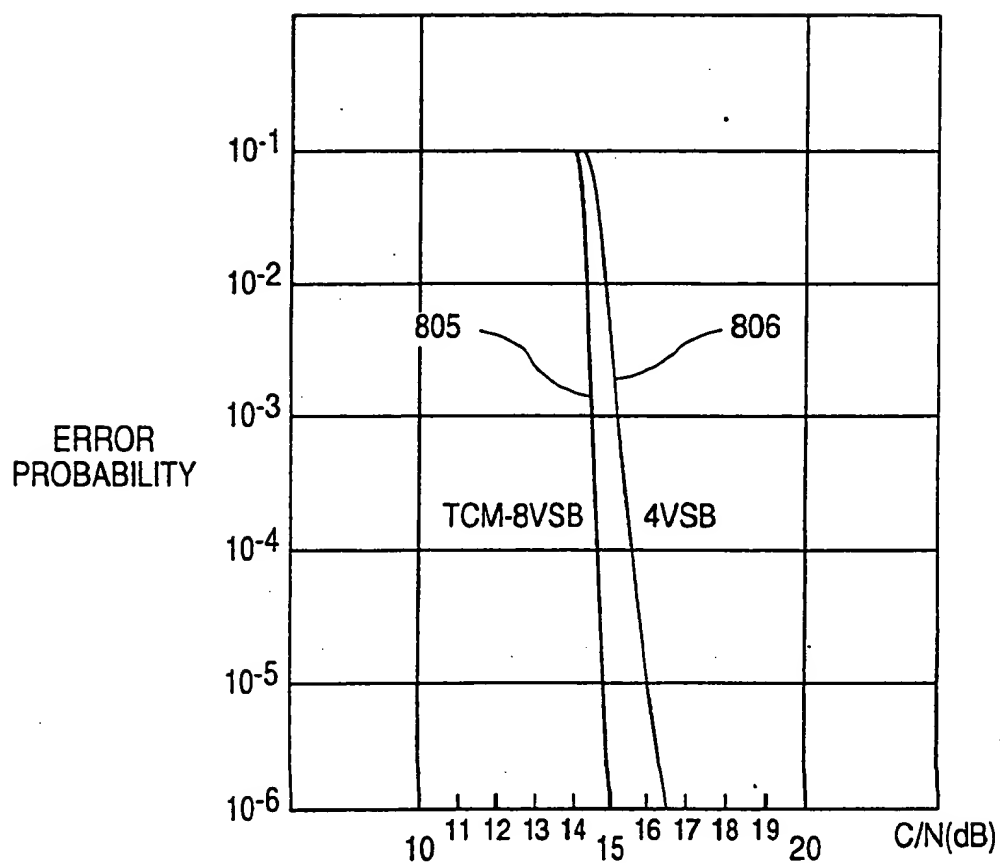


FIG. 163



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FIG. 164

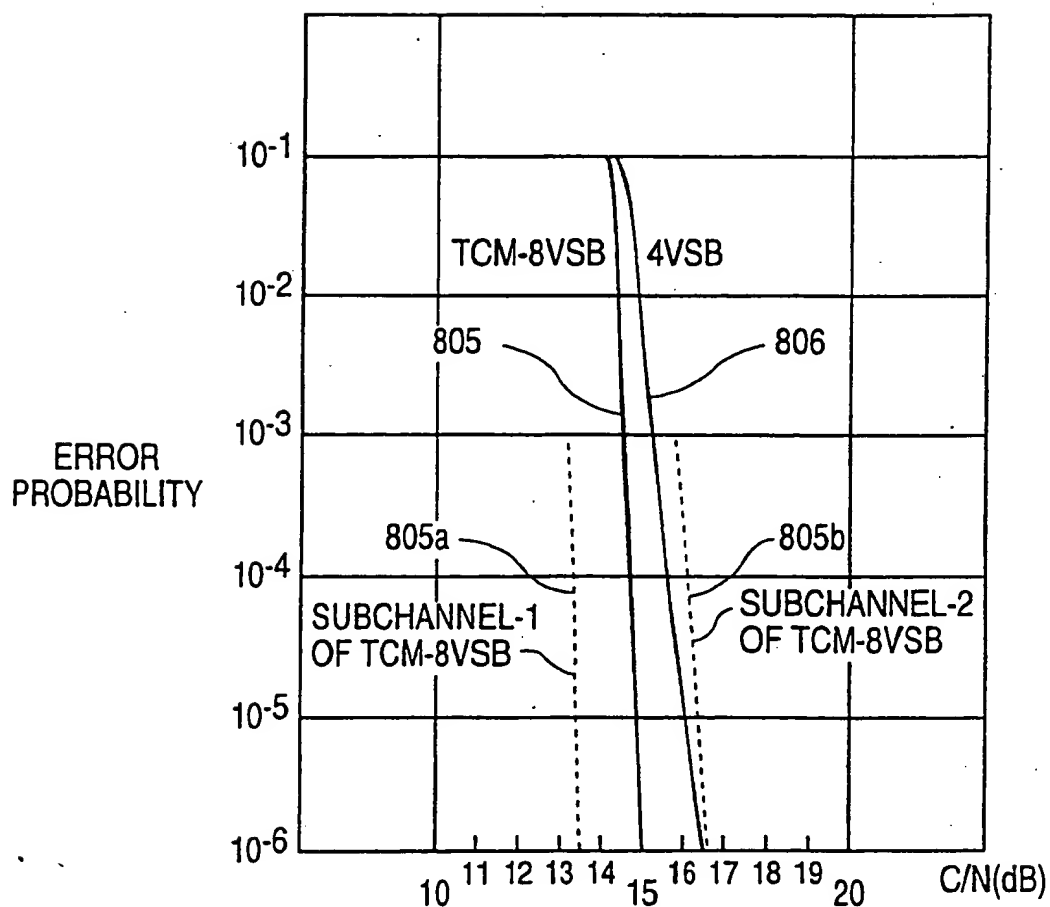


FIG. 165(a)

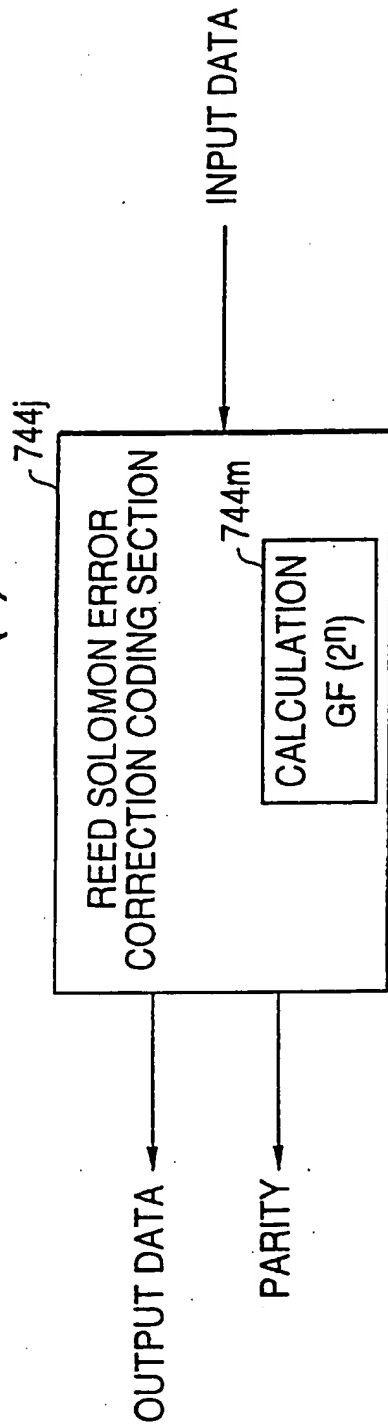


FIG. 165(b)

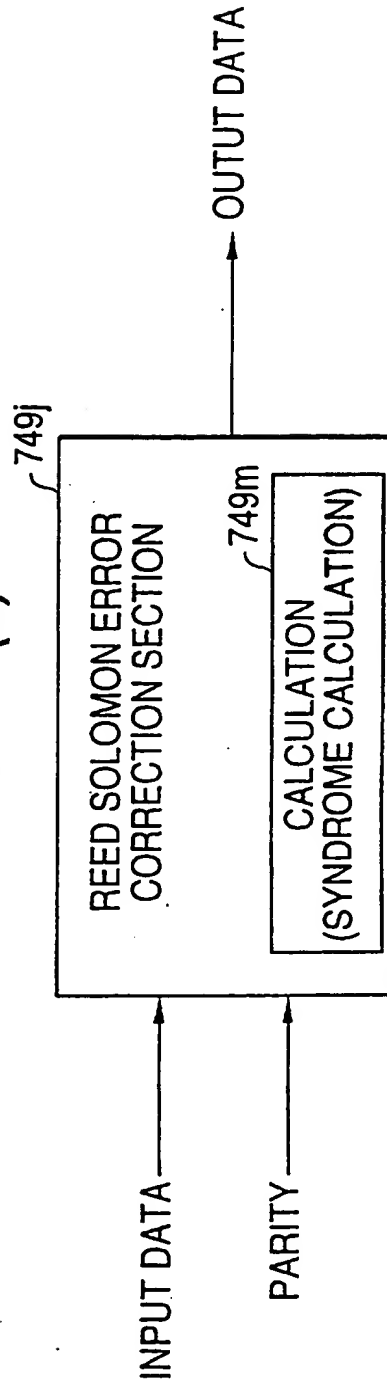


FIG. 166

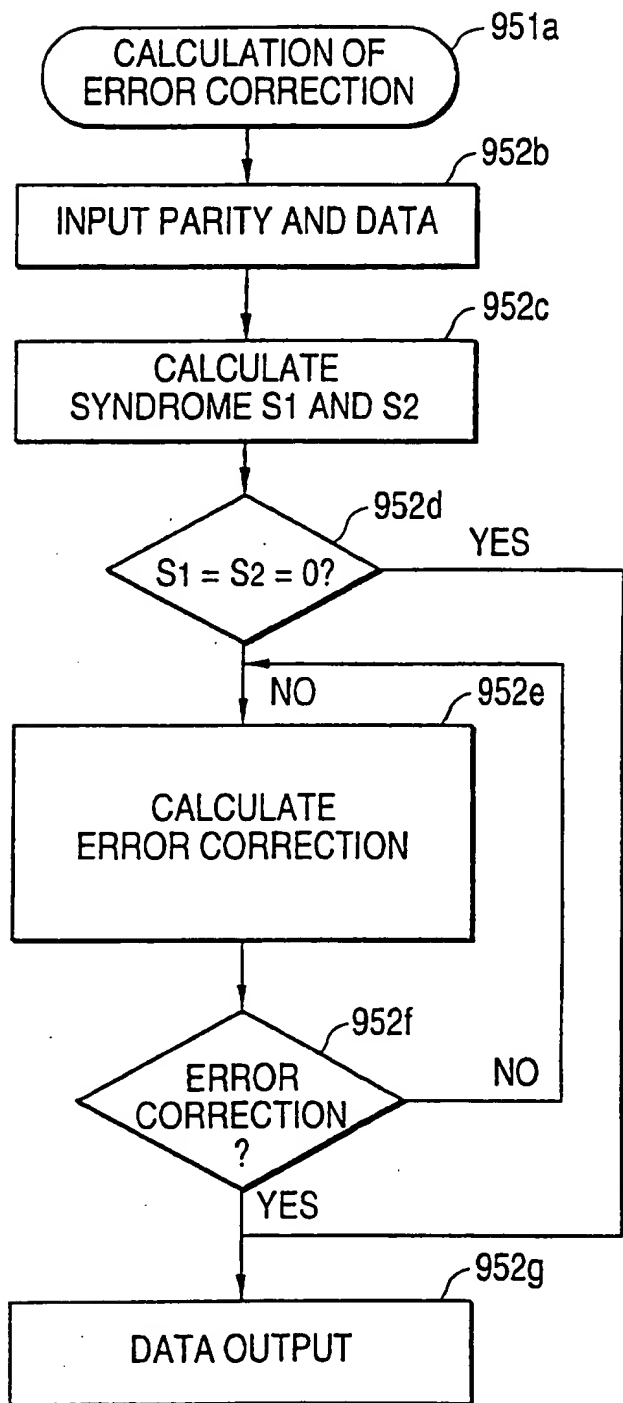


FIG. 167

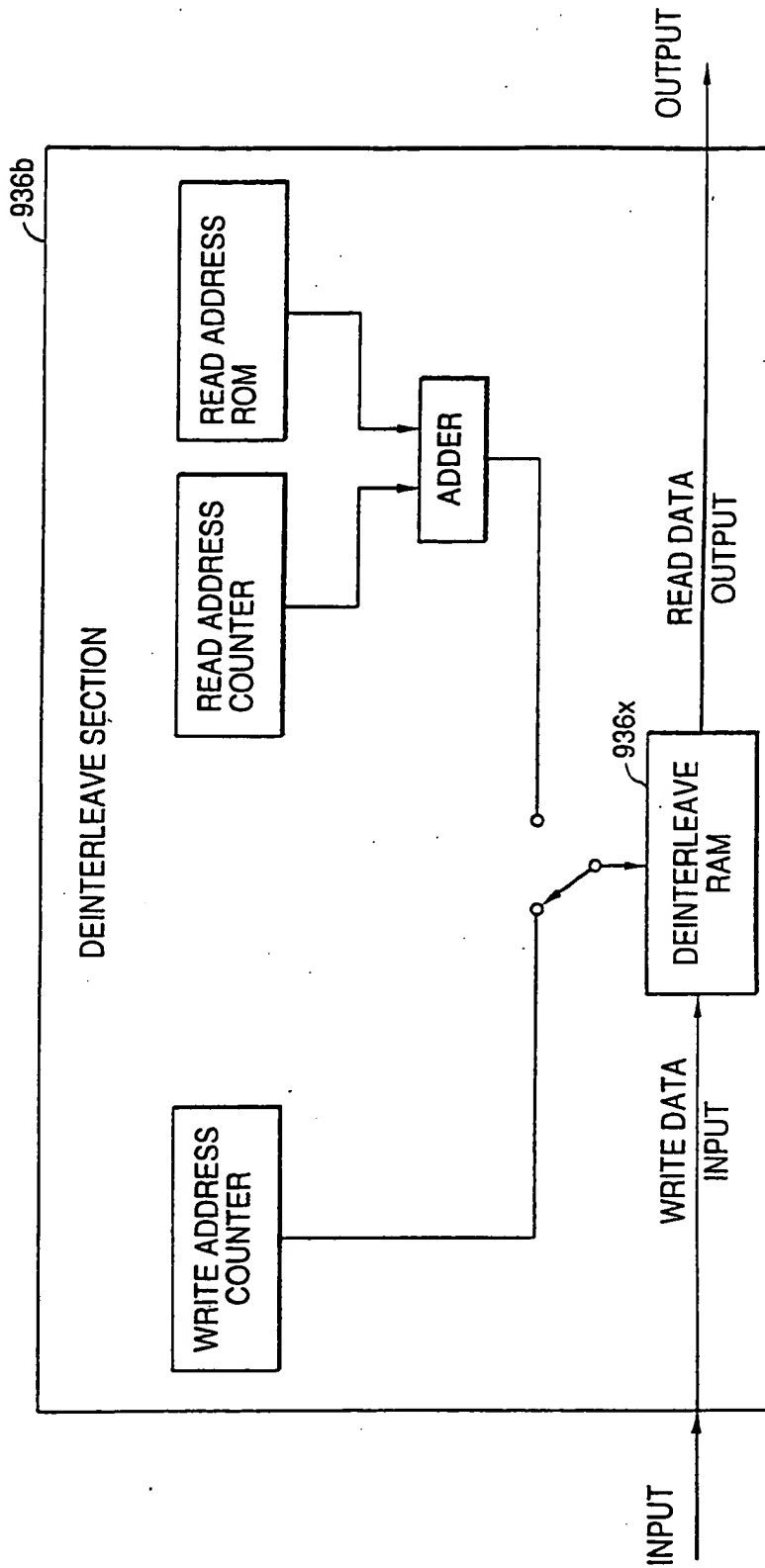


FIG. 168(a)

INTERLEAVE TABLE

DATA							954
1	2	3	4	5	6	7	C2 PARITY
1	A 1	A 2	A 3	A 4	A 5	A 6	PARITY
2	B 1	B 2	B 3	B 4			
3	C 1						
4	D 1						
5	E 1						
6	F 1						
C1 PARITY	PARITY	PARITY	PARITY	PARITY	PARITY	PARITY	PARITY

951b

951a

953

FIG. 168(b)

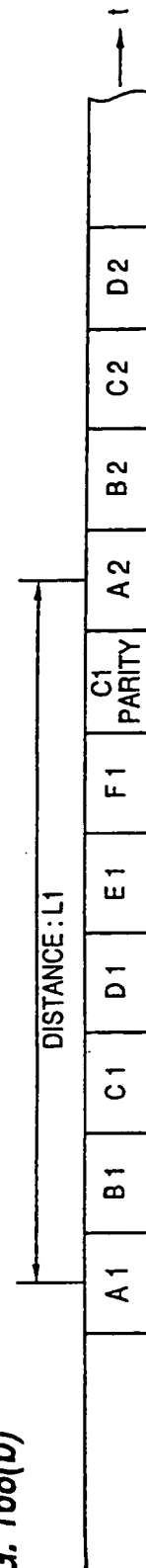


FIG. 169

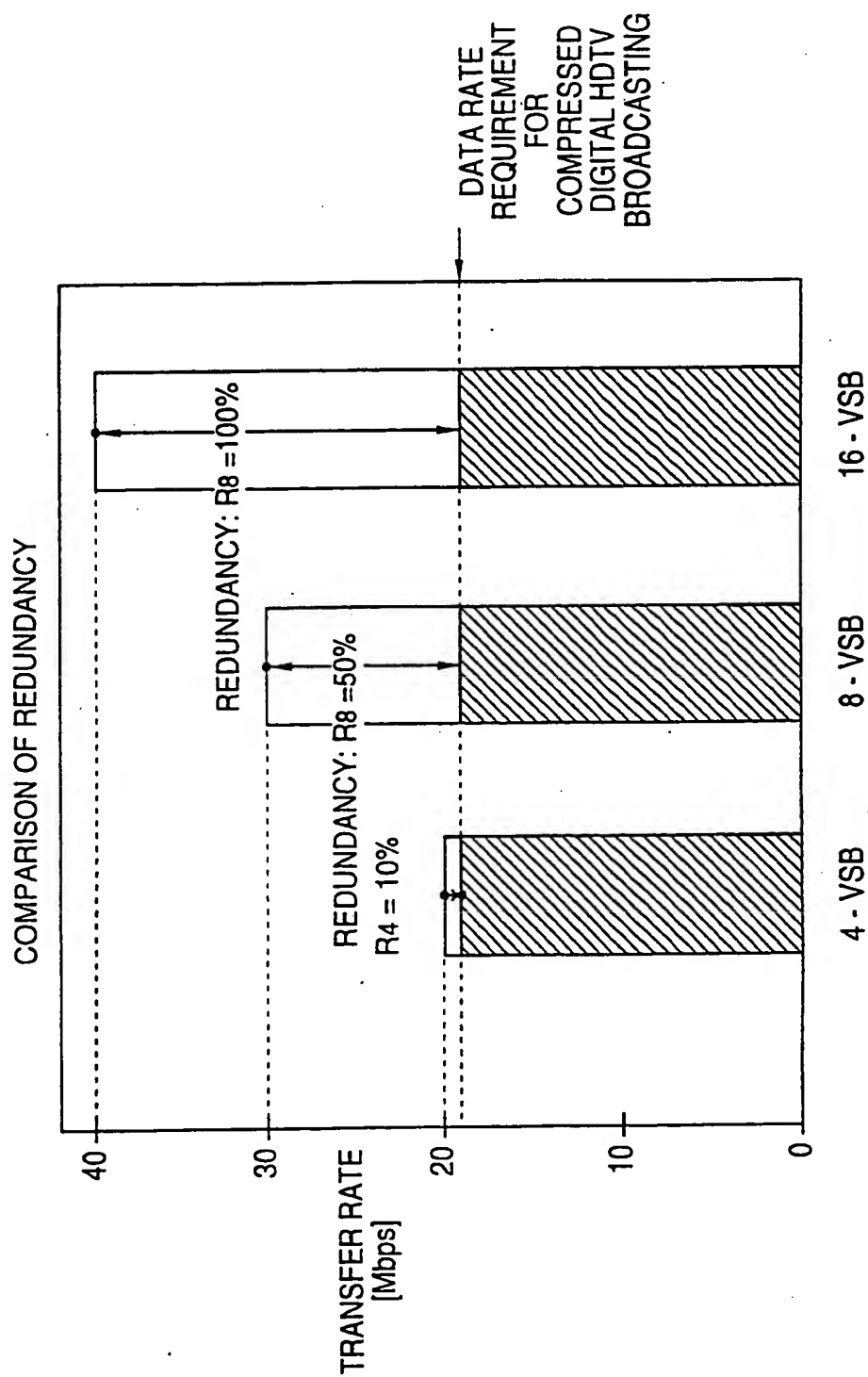


FIG. 170

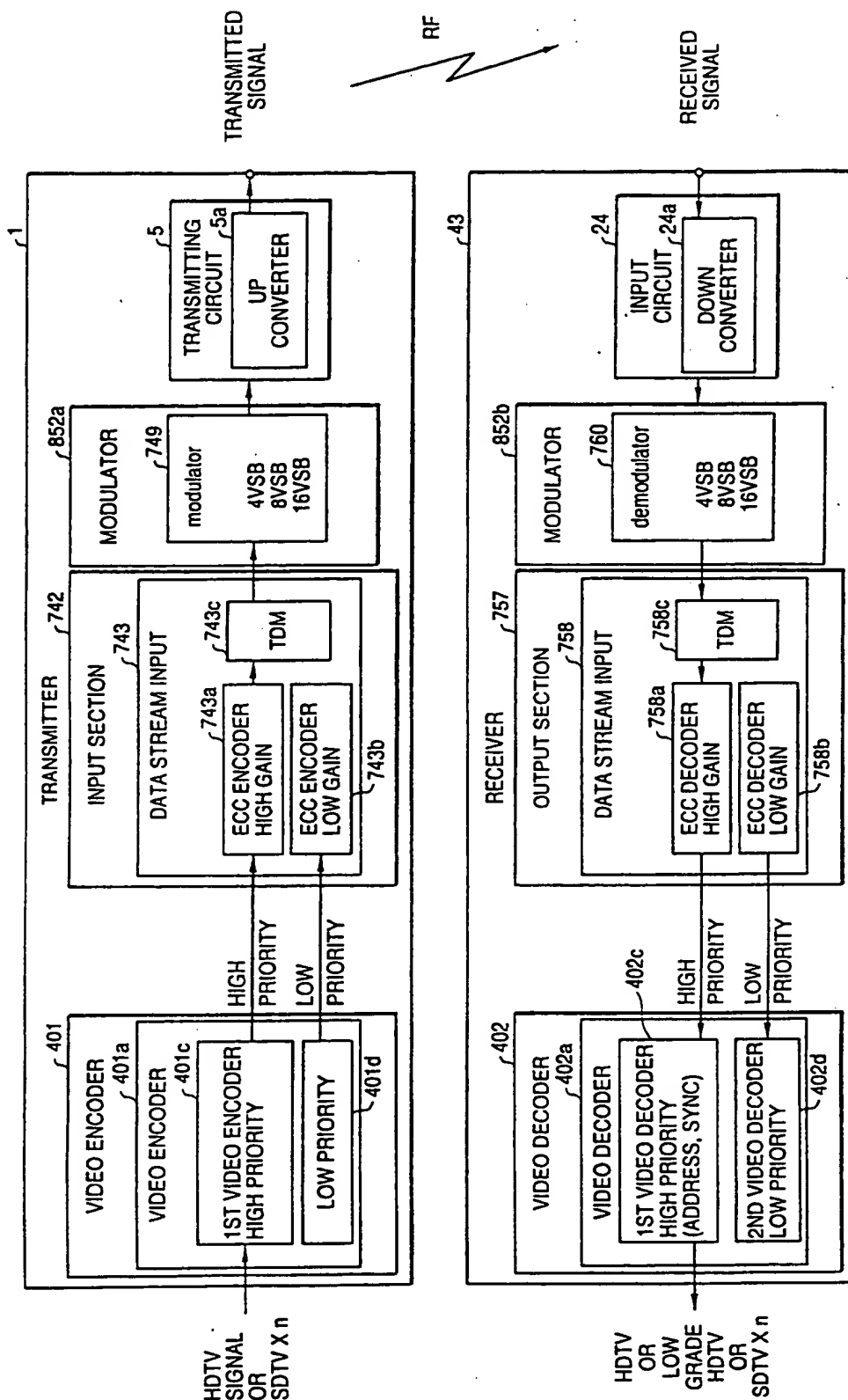


FIG. 171

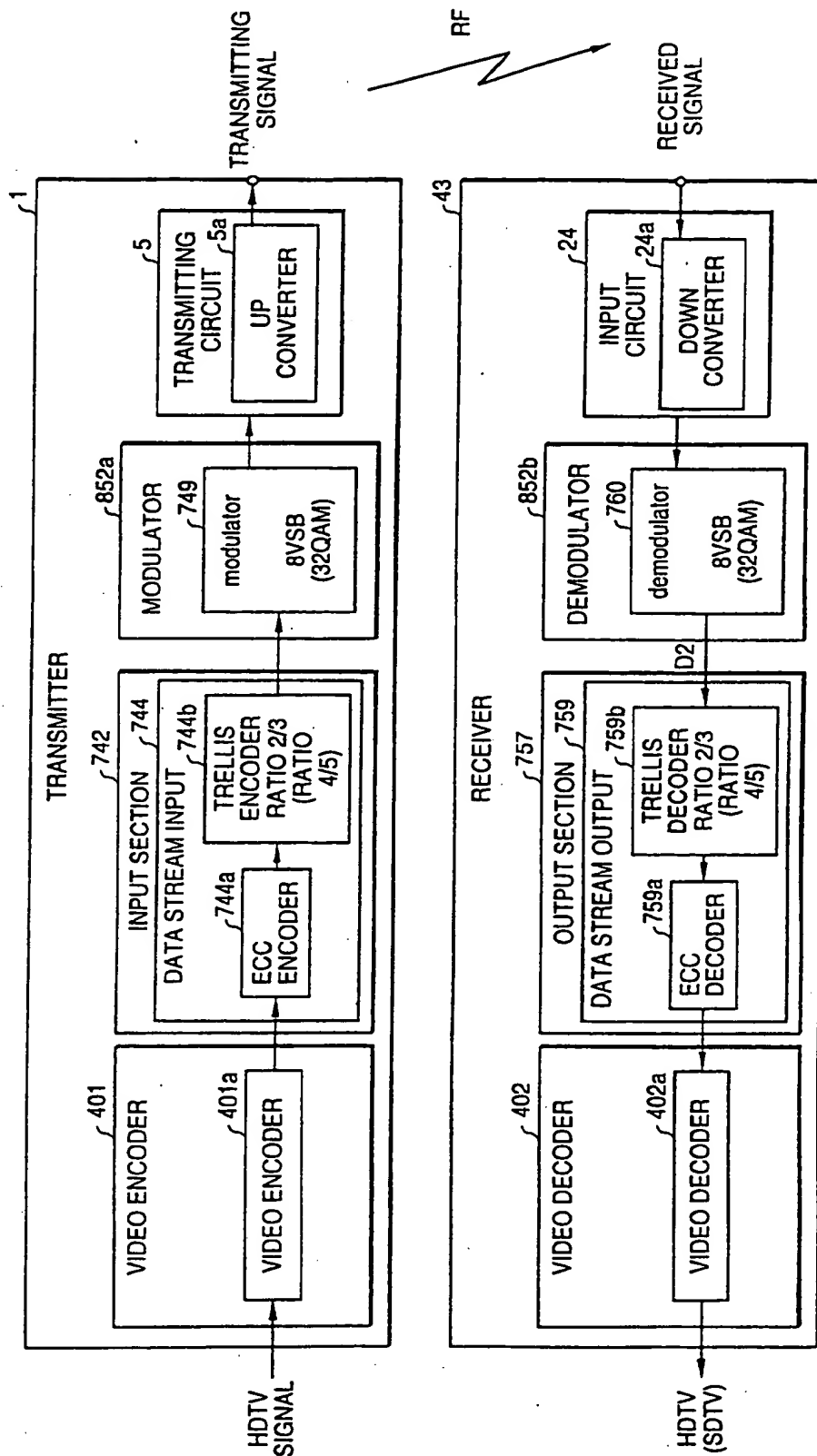
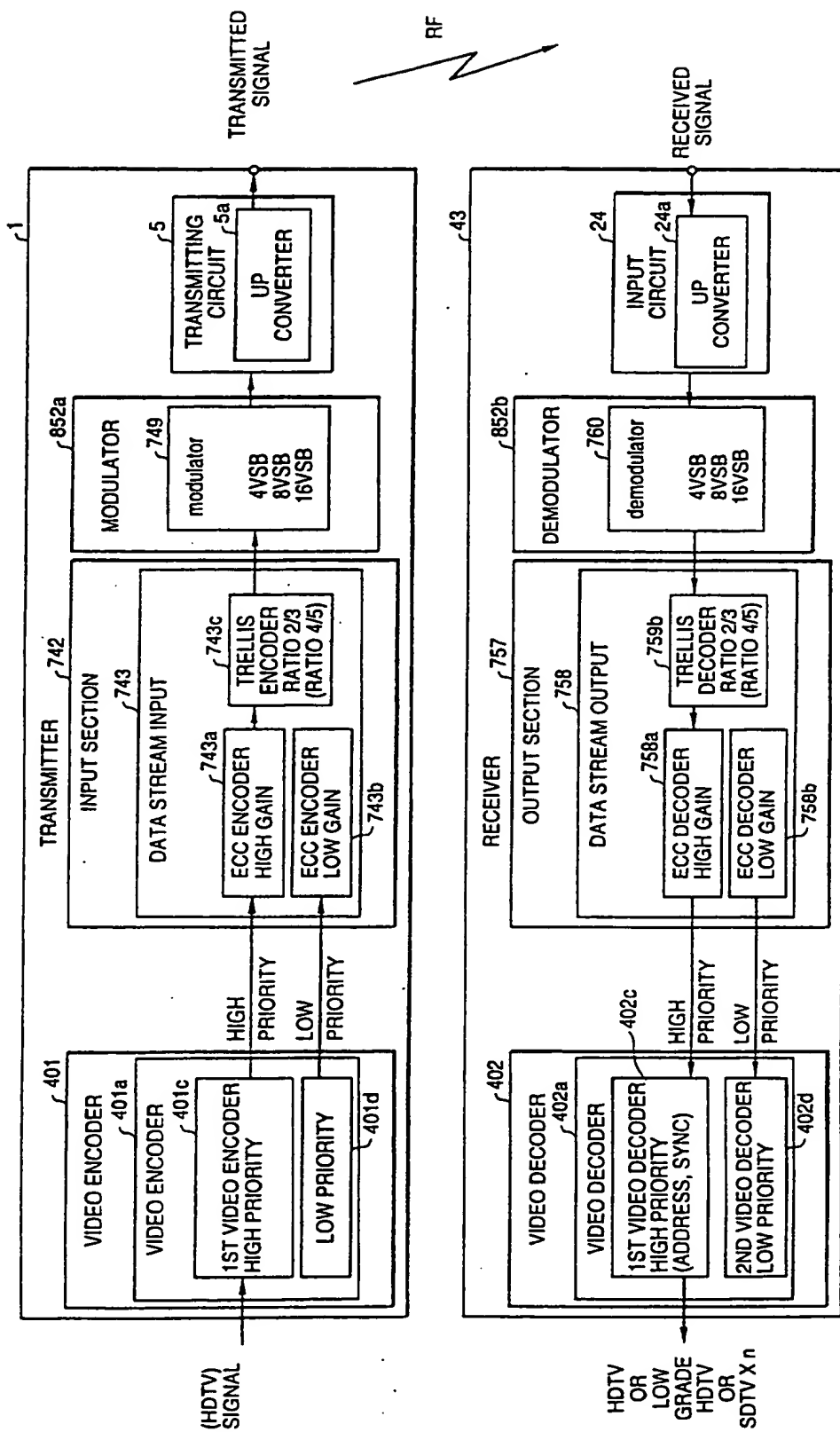
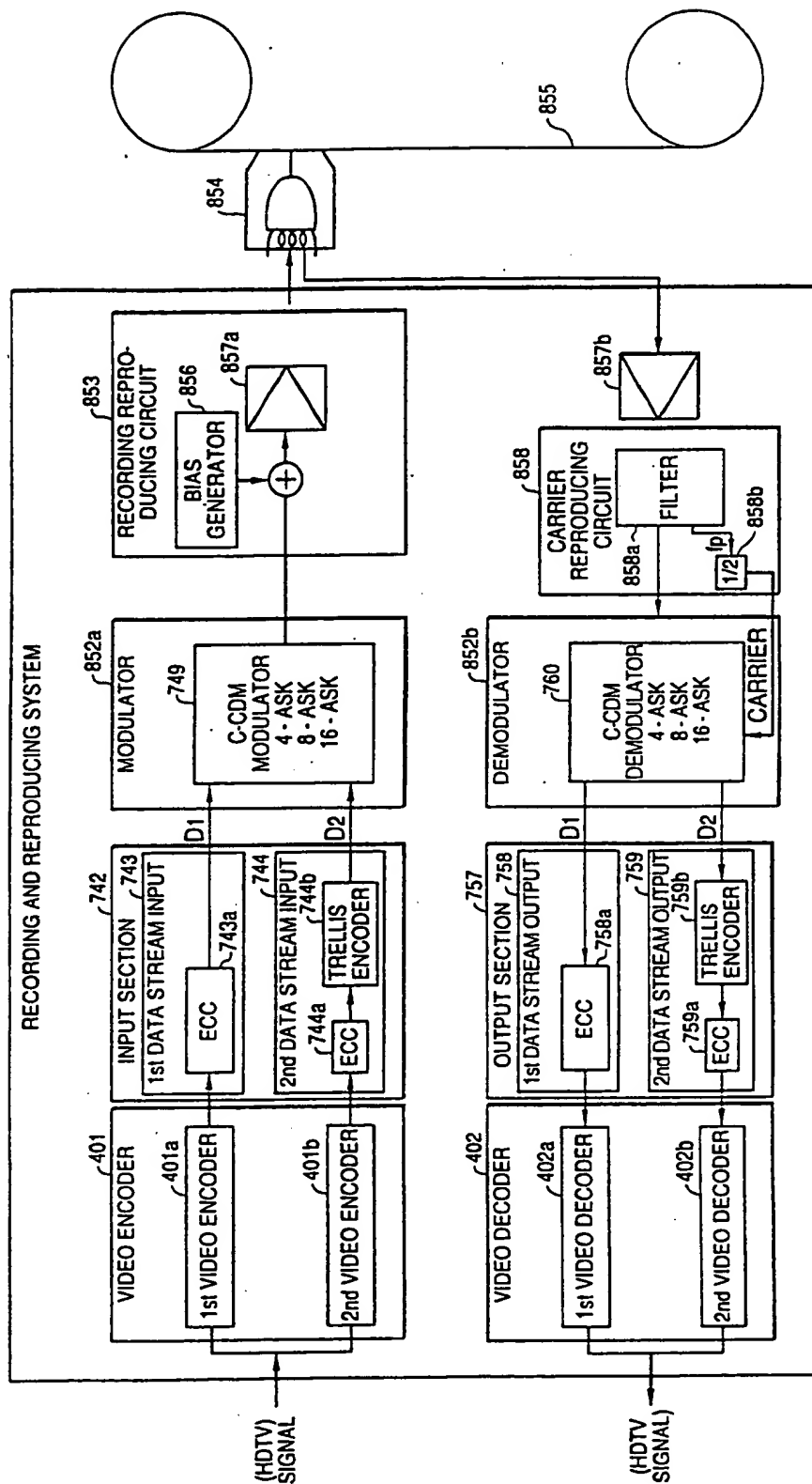


FIG. 172





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FIG. 174

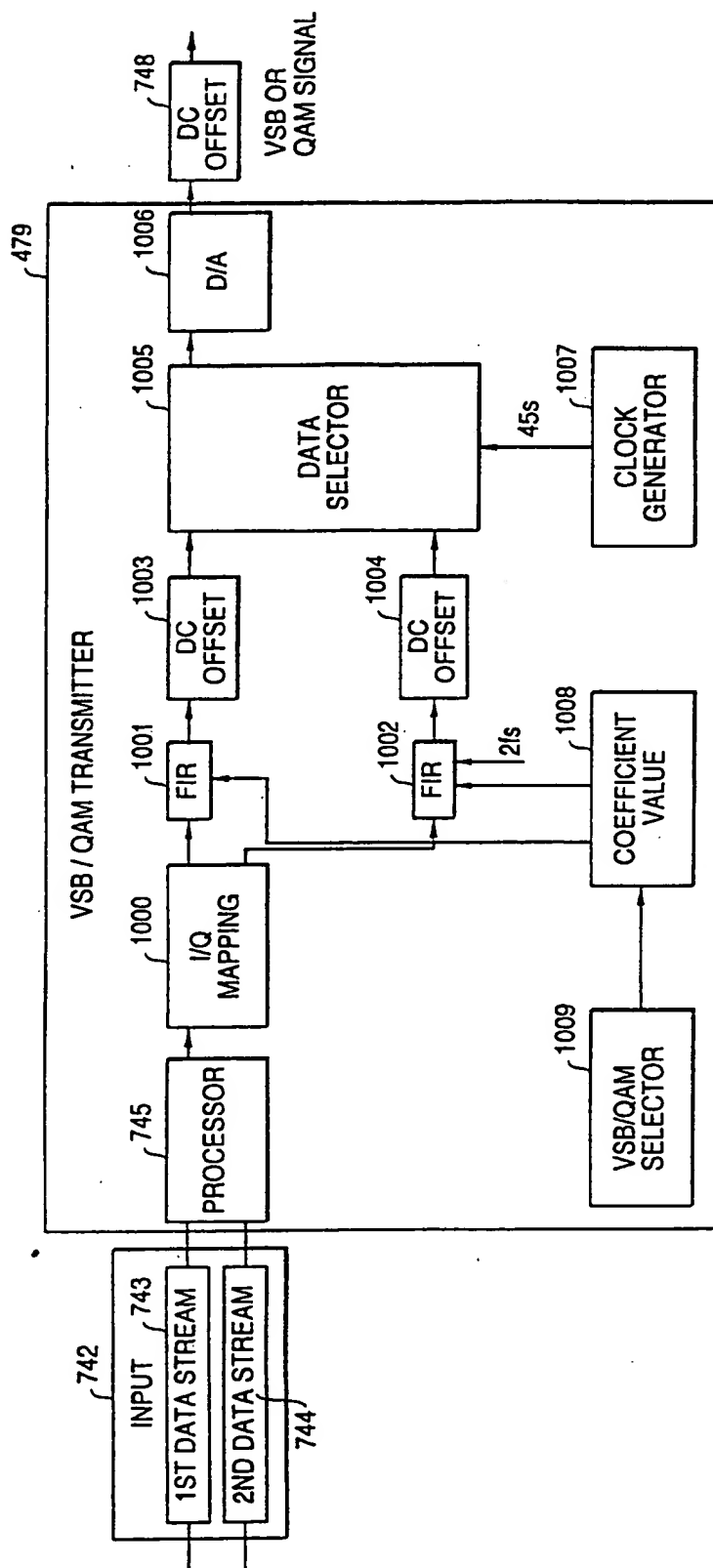
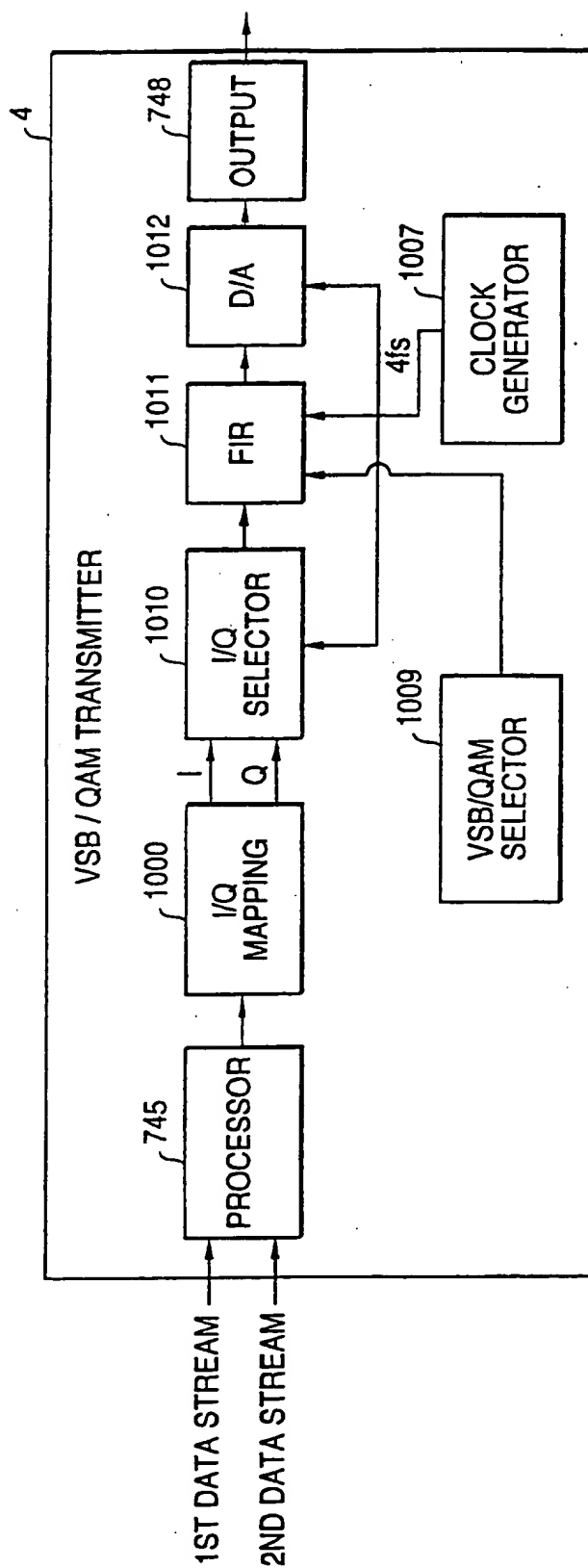


FIG. 175



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FIG. 176

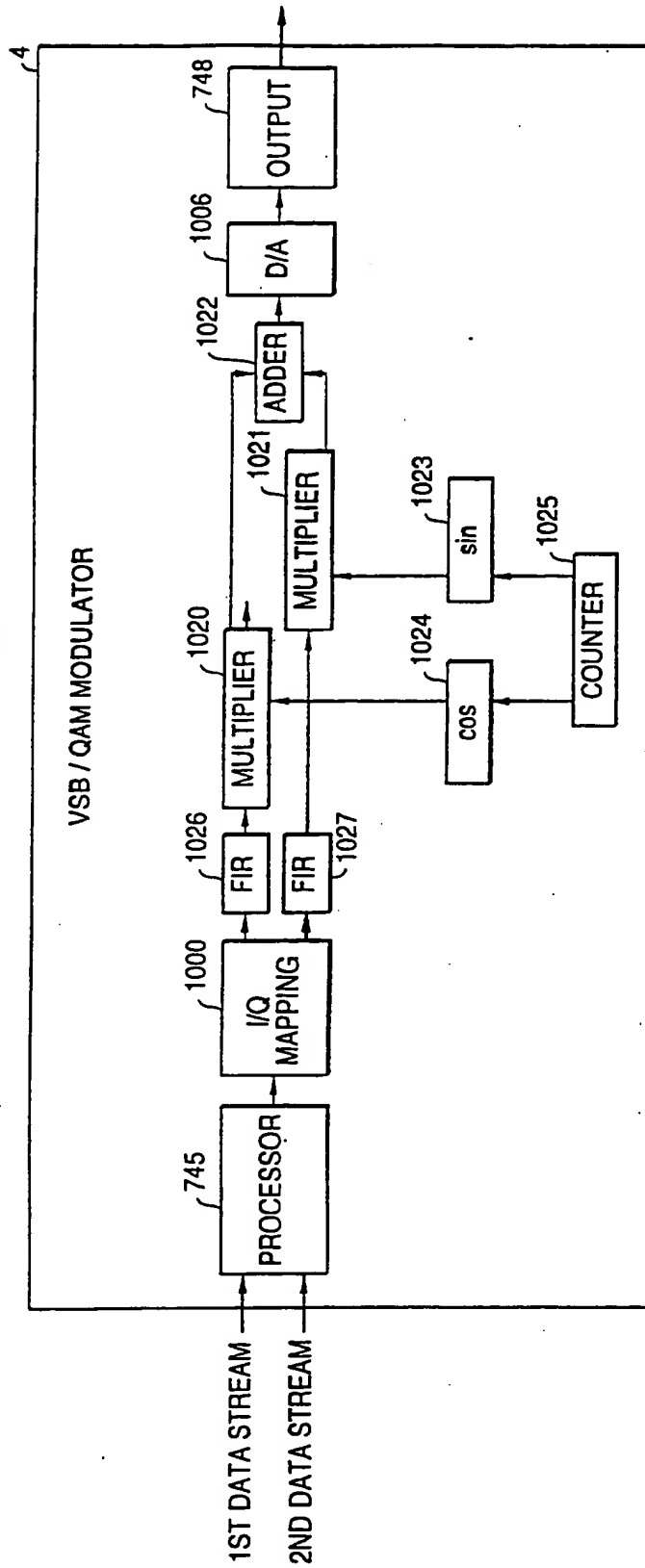


FIG. 177

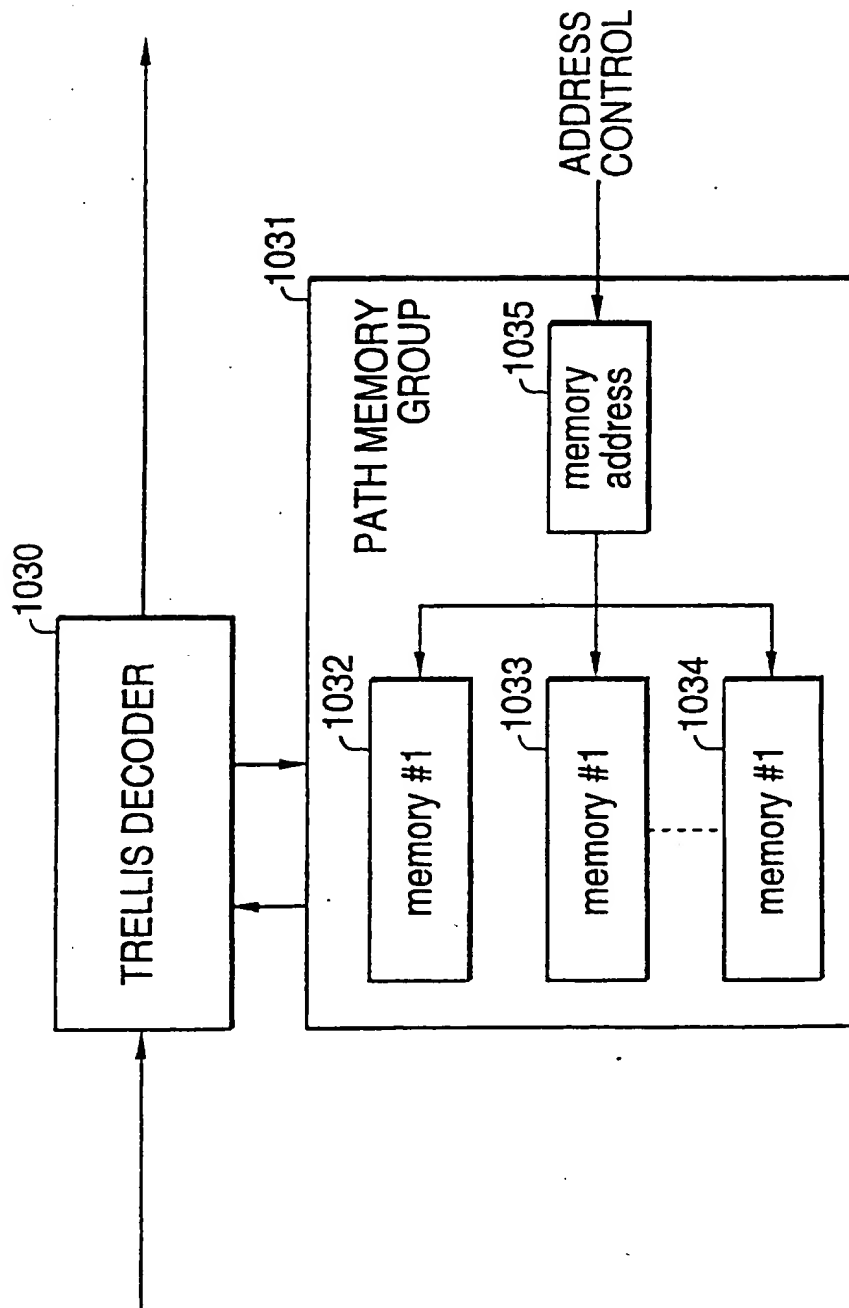
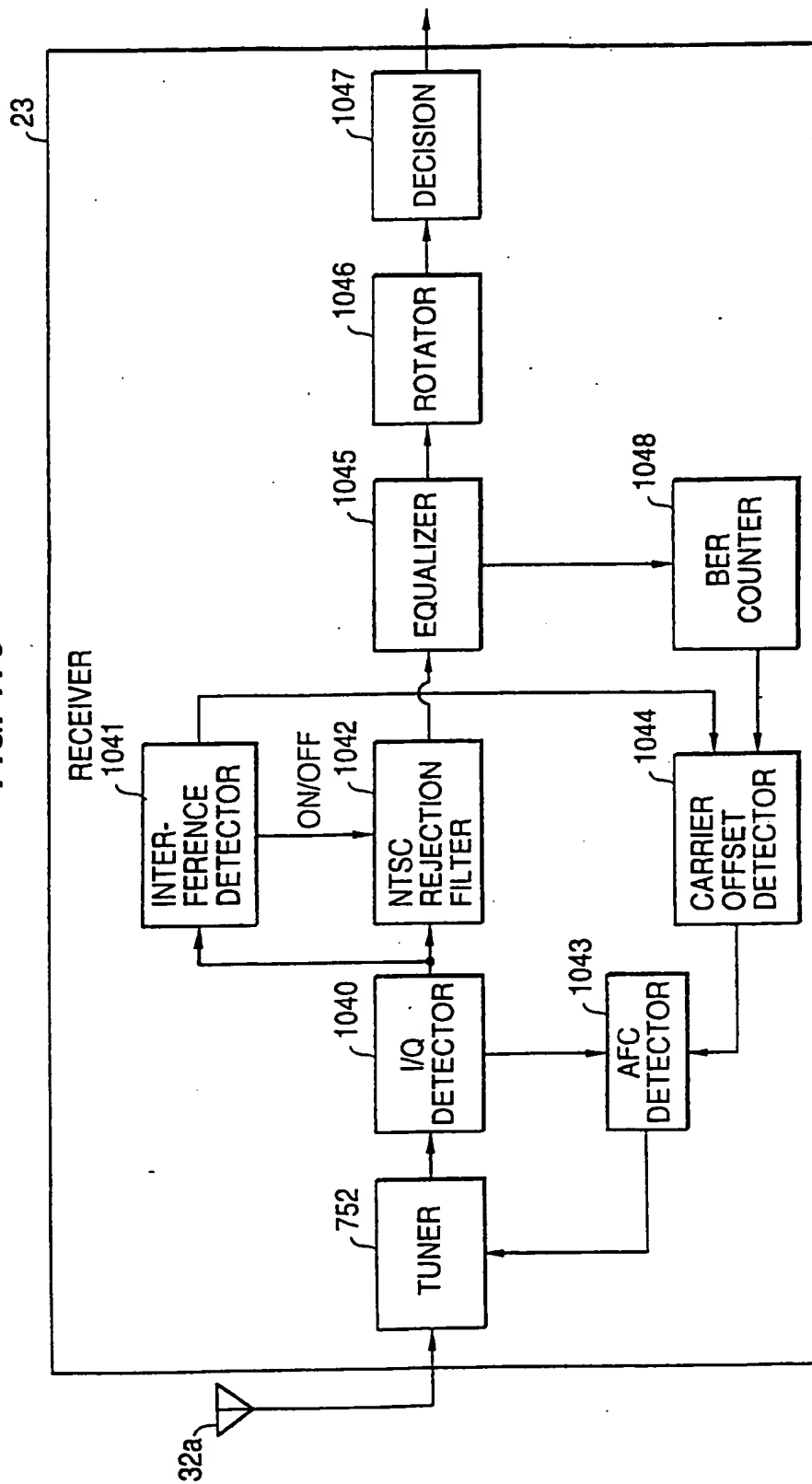
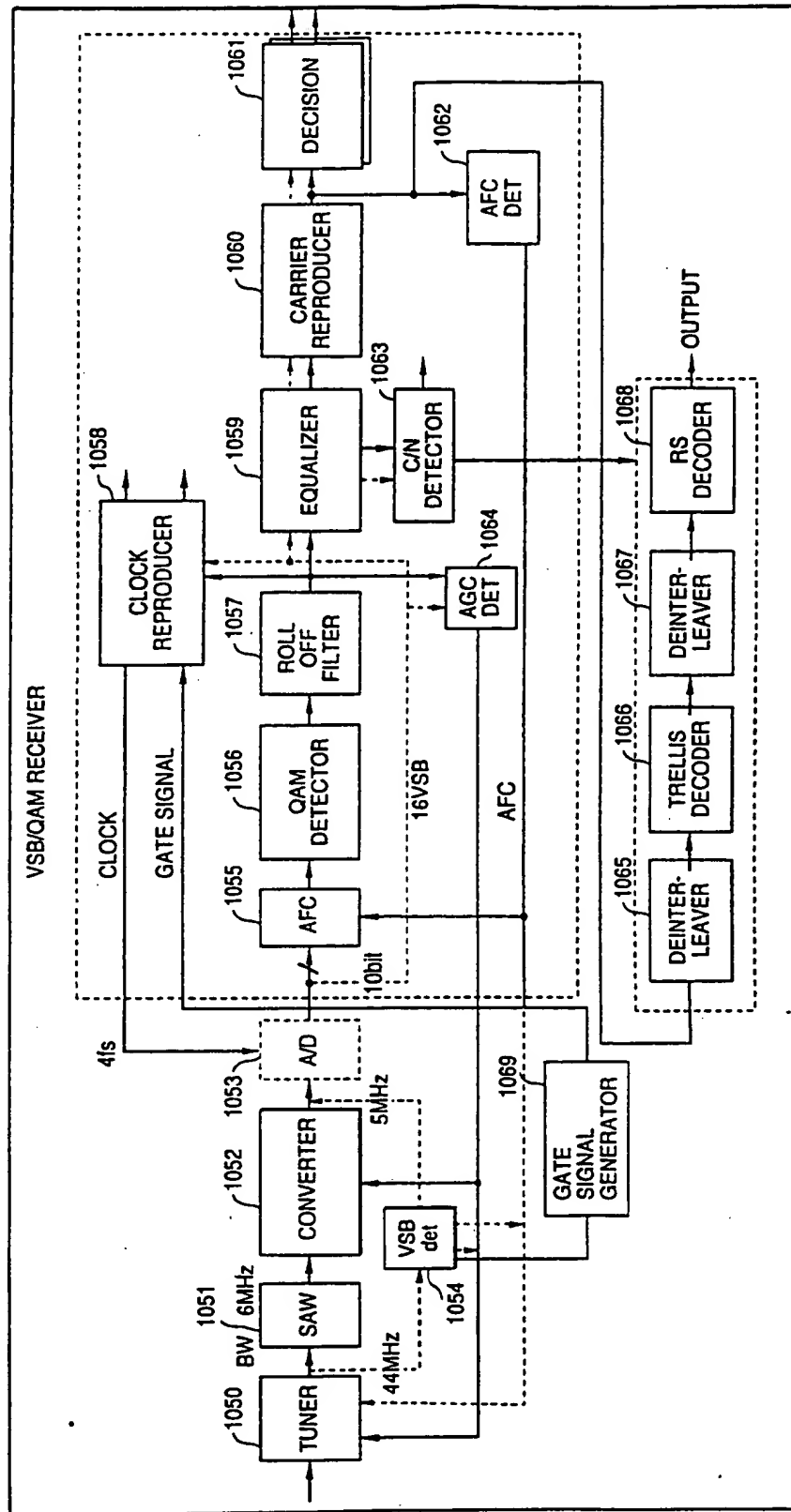


FIG. 178



**FIG. 179**

[illegible]